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POROUS SILICON TECHNOLOGY FOR INTEGRATED MICROSYSTEMS

by

Jin Zheng Wallner

A DISSERTATION

Submitted in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

(Electrical Engineering)

MICHIGAN TECHNOLOGY UNIVERSITY

2006

This dissertation, “Porous Silicon Technology for Integrated MicroSystems,” is hereby approved in partial fulfillment of the requirements for the degree of doctor of philosophy in the field of Electrical Engineering.

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ABSTRACT

POROUS SILICON TECHNOLOGY FOR INTEGRATED MICROSYSTEMS

by Jin Zheng Wallner

With the development of micro systems, there is an increasing demand for integrable porous materials. In addition to those conventional applications, such as filtration, wicking, and insulating, many new micro devices, including micro reactors, sensors, actuators, and optical components, can benefit from porous materials. Conventional porous materials, such as ceramics and polymers, however, cannot meet the challenges posed by micro systems, due to their incompatibility with standard micro-fabrication processes. In an effort to produce porous materials that can be used in micro systems, porous silicon (PS) generated by anodization of single crystalline silicon has been investigated.

In this work, the PS formation process has been extensively studied and characterized as a function of substrate type, crystal orientation, doping concentration, current density and surfactant concentration and type. Anodization conditions have been optimized for producing very thick porous silicon layers with uniform pore size, and for obtaining ideal pore morphologies. Three different types of porous silicon materials: meso porous silicon, macro porous silicon with straight pores, and macro porous silicon with tortuous pores, have been successfully produced. Regular pore arrays with controllable pore size in the range of $2\mu\text{m}$ to $6\mu\text{m}$ have been demonstrated as well. Localized PS formation has been achieved by using oxide/nitride/polysilicon stack as masking materials, which can withstand anodization in hydrofluoric acid up to twenty hours. A special etching cell with electrolytic liquid backside contact along with two process flows has been developed to enable the fabrication of thick macro porous silicon membranes with through wafer pores. For device assembly, Si-Au and In-Au bonding technologies have been developed. Very low bonding temperature ($\sim 200^\circ\text{C}$) and thick/soft bonding layers ($\sim 6\mu\text{m}$) have been achieved by In-Au bonding technology, which is able to compensate the potentially rough surface on the porous silicon sample without introducing significant thermal stress.

The application of the porous silicon material in micro systems has been demonstrated in a micro gas chromatograph system by two indispensable components: an integrated vapor source and an inlet filter, wherein porous silicon performs the basic functions of porous media: wicking and filtration. By utilizing a macro porous silicon wick, the calibration vapor source was able to produce a uniform and repeatable vapor generation for n-decane with less than a 0.1% variation in 9 hours, and less than a 0.5% variation in rate over 7 days. With engineered porous silicon membranes the inlet filter was able to show a depth filtration with nearly 100% collection efficiency for particles larger than $0.3\mu\text{m}$ in diameter, a low pressure-drop of 523Pa at 20sccm flow rate, and a filter capacity of $500\mu\text{g}/\text{cm}^2$.

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Chapter 1

Introduction

Since the birth of the first silicon based pressure sensor in late 1950s, MicroElectro-Mechanical System (MEMS) technology has been enjoying continual prosperity. Micromachined devices, including ink-jet print heads, magnetic disk heads, pressure sensors, accelerometers, uncooled infrared imaging devices and projection displays, have been successfully fabricated to deliver good performance at very low cost [1].

However, there is still plenty room at the bottom [2]. Scientists and engineers through out the world are working on developing even more complex micro systems, from micro robots to a lab-on-a-chip. One of the leading research organizations that is dedicated to this effort is the Engineering Research Center (ERC) for Wireless Integrated MicroSystems (WIMS), a partnership among the University of Michigan, Michigan State University, Michigan Technological University, and member companies [3]. The goal of the WIMS center is to merge sophisticated ensembles of micro sensors and micro instruments with embedded micro controllers and micro mechanical wireless transceivers into functional micro systems that only occupy volumes of $\sim 1\text{cm}^3$ and operate at a few mW of power [4]. Two testbeds have been chosen as research foci. The first is a neural prosthesis testbed. It utilizes different configurations of implantable silicon probes to electrically stimulate the nerve system, to record neural signals, and to deliver drugs. Equipped with on-board electronics, insertion tools, a wireless link and an external microcontroller, this testbed can be used to evaluate a variety of new approaches to the management of neurological dis-

orders, such as deafness, epilepsy, and Parkinson's disease. The second testbed is a multi-component environmental monitor for parameters such as ambient pressure, temperature, humidity, radiation, and air/water contaminants [4]. The centerpiece of this testbed is a micro gas chromatograph (μ GC) that is capable of *in-situ* determination of mixtures of up to 30–50 vapors at low- or sub-part-per-billion (ppb) levels in a single 10–20 minute analysis. With an embedded microcontroller and RF communication modules, the ultimate product can be deployed in high-performance distributed environmental monitoring networks.

The development of the two extremely complex testbeds is driving research in every aspect of micro systems, from materials to processes and technology integration. For example, various functional materials, including single crystal PZN-PT films, poly-C (diamond) films, silicon carbide, metal nanoclusters, and carbon nanotubes, have been developed for or applied to the testbeds for sensing, actuation, or packaging. This thesis work concerns a particular type of material for the testbeds: porous materials. In the macro world, porous materials have already been widely used in industry and households for centuries. Well-engineered porous materials of different properties are commercially available to serve various roles, such as filters, electrodes, insulators, structural materials, etc. Similar to the macro world, porous materials are also needed in micro systems. Here, in addition to its conventional functions, there are many new applications for porous materials, such as micro reactors, sensors, and optical components. However, micro systems pose new challenges to porous materials. The fabrication techniques of conventional porous materials, such as ceramics and polymers, are not compatible with standard micro-fabrication processes. The lack of scalability and micro-manufacturability along with the difficulty of integration limits the use of conventional porous materials in micro systems. Therefore, new types of porous materials and supporting technologies are needed to meet the fast growing demand of porous materials in micro systems.

1.1 Motivations and Goals

As a technology development project for the testbeds, the main goal of this research work is to produce porous materials that are scalable, integrable, versatile, and therefore suitable for micro systems. There are several components in the two WIMS testbeds that may benefit from porous materials. One of them is the internal vapor standard, which can generate vapor with known concentration to calibrate and maintain the performance of the μ GC. A second one is the inlet filter, which removes particles from the gas samples for the μ GC. A third one is the electro-osmotic pump for hydraulic actuation in the prosthesis testbed. Although porous membranes and porous silica blocks are commercially available and are well established in the use of macro scale devices, they are too fragile to be machined into micro scale parts; not to mention batch producing them, packaging them and interfacing them with other micro devices. In this thesis work, porous silicon (PS) generated by anodization of single crystalline silicon was chosen as the subject of investigation due to its diversity in morphologies, its compatibility with micro-fabrication processes, and its chemical compatibility with the organic vapors. Various porous silicon materials have been developed to address the issue of integrating porous materials into the testbeds. The versatility of the porous silicon material will be demonstrated in the internal vapor standard and the inlet filter, wherein porous silicon performs the basic functions of a porous material: filtration and wicking. The specific objectives of this project include:

- Design and build the experimental system, including hardware and software, for forming porous silicon.
- Study the process parameters, such as electrolyte composition, substrate orientation, doping concentration, illumination, etc. for porous silicon formation. Understand the impact of the parameters on the film morphology, pore size, porosity, and etching rate.

- Optimize porous silicon material for each application.
- Develop supporting technologies, such as localized formation of PS, bonding, and membrane formation, for integrating and packaging the porous silicon material.
- Fabricate devices with the optimized porous silicon materials.
- Obtain testing results for the final devices.

1.2 Dissertation Outline

This dissertation starts with a background chapter. It gives a brief introduction of the WIMS μ GC, especially the calibration vapor source and inlet filter, for which the porous silicon materials in this research were developed. The roles of porous silicon in both devices will be identified there. It also gives a brief review of porous silicon technology – its unique properties and some established applications. Chapter 3 describes the development of porous silicon materials at MTU, beginning with an introduction of porous silicon formation mechanisms. Followed by a detailed description of the experimental setup for porous silicon formation. Chapter 3 concludes with a discussion of the development and optimization of three types of porous silicon. Chapter 4 details the development of supporting technologies that address the integration issues of porous silicon material in micro systems. The next two chapters cover the design, fabrication, and testing of both devices. Chapter 5 is dedicated to the calibration vapor source and chapter 6 is dedicated to the inlet filter. Finally, Chapter 7 summarizes the findings of this research and presents suggestions for future study.

Chapter 2

Background

2.1 WIMS μ GC

Gas chromatography is the most widely used method for the analysis and characterization of mixtures of volatile and semivolatile organic compounds. A generalized schematic of a traditional GC is shown in Figure 2.1. The analyte mixture is injected into the column in a narrow pulse. As gas molecules travel through the column with the carrier gas, the velocities are determined by their interactions with the solid phase in the column. If the differences in velocities are sufficient or the column is long enough, a complete separation of each component is possible [7]. The resolved vapors

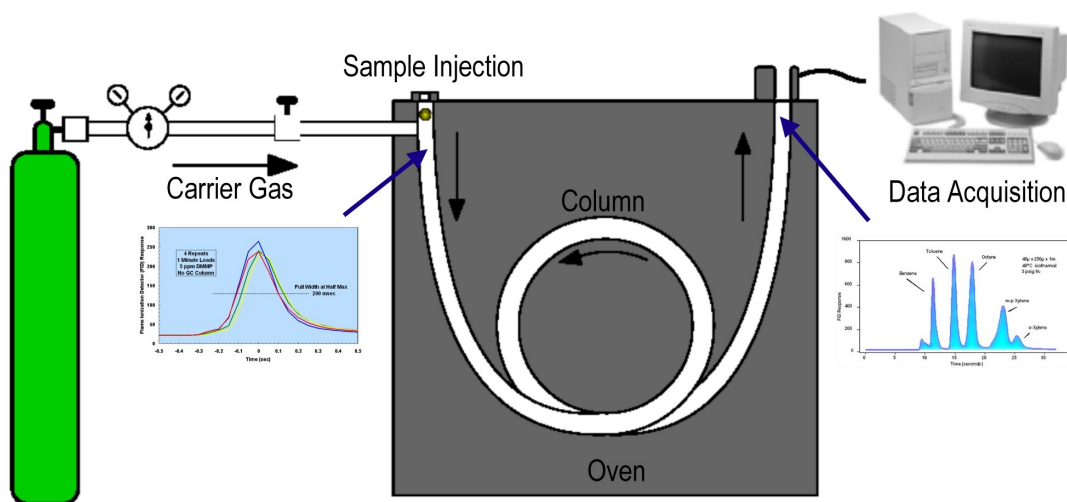


Figure 2.1: Generalized schematic of a GC system (adapted from [5,6])

are then detected by GC detectors, such as Flame Ionization Detector (FID), Thermal Conductivity Detector (TCD), or Mass Spectrometer (MS), as they exit the GC column. The requirements of a GC detector depends on the separation application. For example, the FID is based on the production of ions in a flame that results in a current that can be measured. It is extremely sensitive with a large dynamic range. But it also destroys samples when the vapors pass through the flame. The Thermal Conductivity Detector, however, consists of an electrically-heated wire or thermistor. The temperature of the sensing element depends on the thermal conductivity of the gas flowing around it. When organic molecules displace some of the carrier gas, it causes a change in the thermal conductivity in the gas flow, resulting in a temperature change in the element, which is sensed as a change in resistance. The TCD is not as sensitive as FID, but it is non-specific and non-destructive.

The traditional GC is very bulky ($\sim\text{m}^3$) and expensive ($>\$10,000$) since the carrier gas is usually supplied by compressed gas cylinders or gas generators and a capillary column of 15–30m long is often required to provide adequate separations. This hinders its application in fields that desire low cost, on-site analysis, such as environmental monitoring. To meet the increasing requirements for a small, lightweight and low-maintenance gas chromatograph system, MEMS based μGC s are being developed at the WIMS center [3]. The ultimate goal for the WIMS μGC project is to integrate the functions of a traditional gas chromatograph into a micro-instrument that only occupies 1-2cm³. The conceptual diagram of the WIMS μGC is shown in Figure 2.2.

Figure 2.3 shows the schematic of the WIMS μGC [4]. Instead of using a complex gas management system, an on board vacuum pump is used with ambient air as the carrier gas in this configuration. In operation, air samples are first drawn into the system to trap vapors on the multistage micropreconcentrator (μPCF). After collection of a predetermined sample volume, the μPCF will be resistively heated and the flow reversed to back flush the trapped vapors to the head of the first separation col-

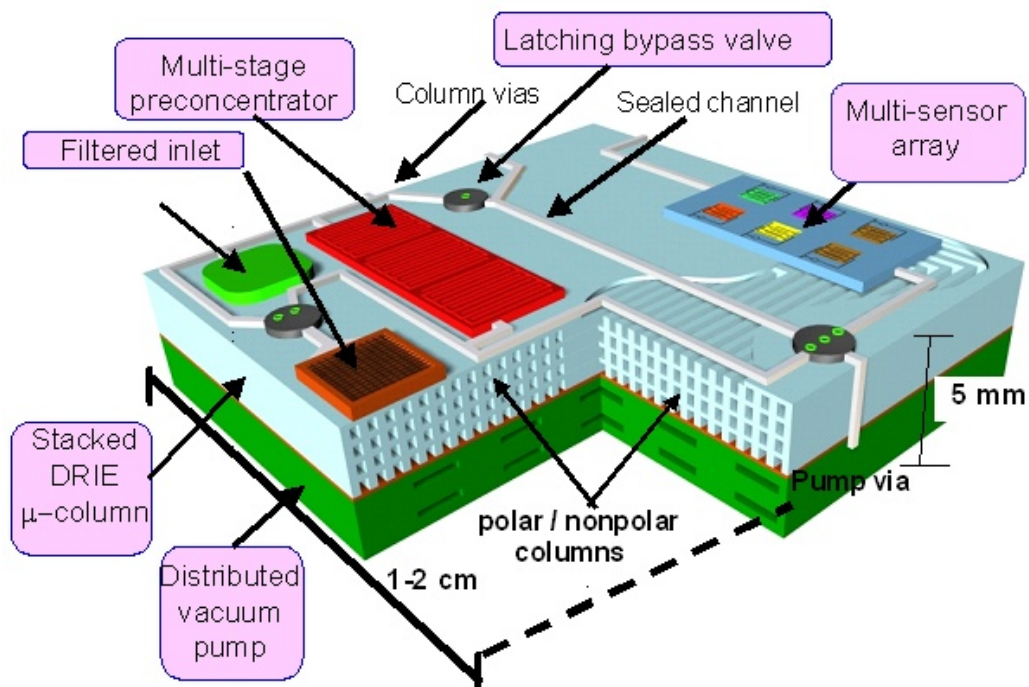


Figure 2.2: Conceptual diagram of the WIMS μ GC [4]

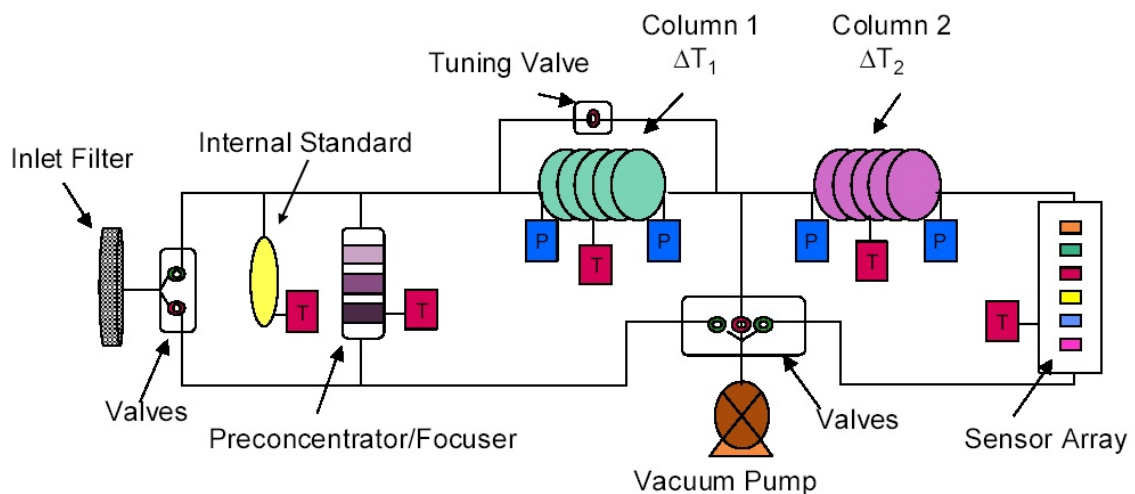


Figure 2.3: Block diagram of key WIMS- μ GC analytical components [4]

umn. The size of the column is also reduced dramatically by using microfabricated columns [8]. Two separation columns with different stationary phases and independent temperature control are being used to optimize the resolution. The resolved or partially resolved vapors are then passed to the sensor array to be detected.

2.2 On-board Calibration Standard for the μ GC

2.2.1 Qualitative and Quantitative Analysis of GC

A gas chromatograph has to be calibrated before any reliable qualitative or quantitative analysis can be performed. Figure 2.4 shows a typical output from a gas chromatograph [9]. Two pieces of data can be obtained from it. The first piece of data is the time for a given component to travel through the column. The definition of absolute retention time t_R , adjusted retention time t'_R and relative retention time $t_{A/B}$ are shown in Figure 2.4. Under a given set of conditions, any component analyzed by gas chromatography has a characteristic retention time. By comparing

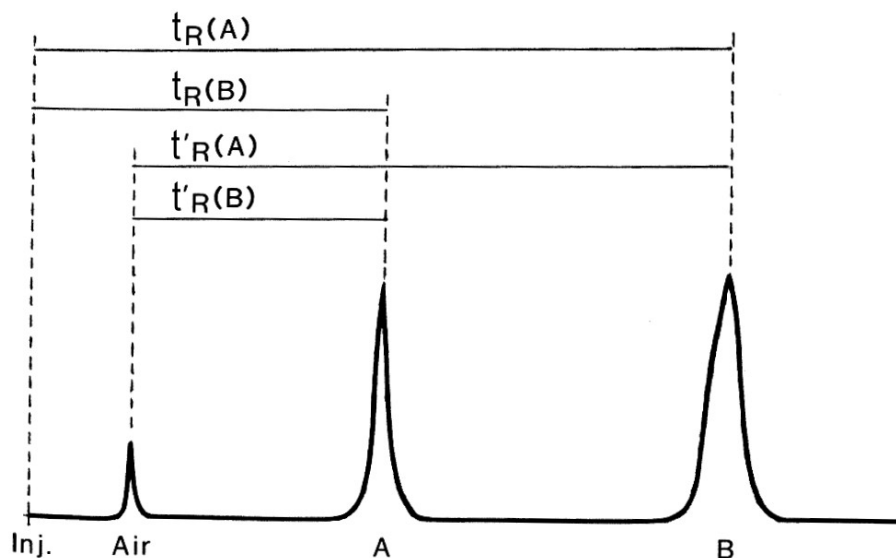


Figure 2.4: Chromatogram illustrating retention nomenclature: t_R = retention time, t'_R = adjusted retention time, $t_{A/B}$ = relative retention time = $t'_R(A)/t'_R(B)$ [9]

the adjusted retention data of an unknown sample with that of a known sample, qualitative analysis can be performed. However, it is difficult to tabulate absolute or adjusted retention times for different columns of the same type. Differences in packing density/coating thickness, age, and previous use of the column will lead to large differences in retention time between two columns. Even for the same column, its condition will change with time and use. This problem can be solved by using relative retention times. The relative retention of a component is its adjusted retention time divided by the adjusted retention time of a standard material. Relative retention data are much less subject to variation in column condition and minor changes in temperature and flow. In Figure 2.4, the standard material is peak B.

The second piece of data is the area under the peak, which is proportional to the amount of material in the sample. To convert the peak area into the measure of the quantity of the material, the gas chromatograph needs to be calibrated with standards of known concentrations. There are three types of calibration techniques.

- External standardization simply creates a chart of relationships between the peak size and the composition of the components of interest by chromatographing standards at the same concentrations as the unknowns in the same matrix as the unknowns. The unknowns can be compared graphically or mathematically to the standards for analysis. A typical calibration curve for four methyl ketones in an air matrix is shown in Figure 2.5, where peak heights were used as the area measurement [9]. It is a lot of work to create and maintain calibration curves. Standards need to be prepared with all components of interest and the range of composition of the standards should cover the entire range expected in the unknowns. To obtain a reliable calibration, the sample size of the standards needs to be the same as the unknowns. And for some applications with rigorous calibration criteria, in addition to running a calibration set before the samples are run, the standard set may need to be interspersed among the samples or

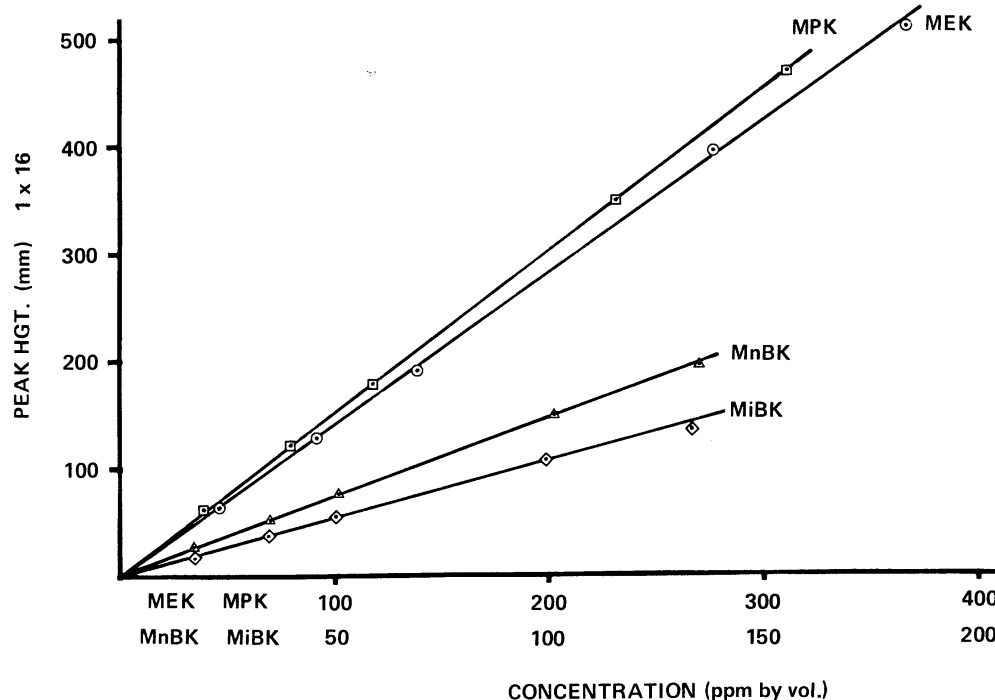


Figure 2.5: Calibration curves for four methyl ketones in an air matrix: 2-butanone (MEK), 2-pentanone (MPK), 2-hexanone (MnBK), 2-methyl,4-pentanone (MiBK) [9]

rerun at the end. All these requirements make it difficult to do the external standardization for on-site analysis.

- Internal normalization can be explained with the example shown in Table 2.1. Ideally, if the detector generates peaks of the same area for different materials of the same weight, the peak areas of all components can be summed and the area percent of each component can be simply used as weight percent of that component in the sample. However, the ideal situation usually doesn't exist. To account for the difference in responses, response factors need to be obtained for all of the components in the sample. A standard is prepared by adding known weights of the pure components to each other and calculating the weight percent as shown in Table 2.1. The standard is then chromatographed and the areas of the four peaks are measured. The area percents are listed as comparisons to the weight percents. The weight percents are then divided by

Table 2.1: Internal normalization [9]

Component	Standard					Response Factor F
	Taken	Weight	Peak	Area	Weight%	
	(g)	(%)	Area	(%)	Area	
A	0.3786	21.74	4231	22.41	0.005138	1.000
B	0.4692	26.94	5087	26.94	0.005296	1.031
C	0.5291	30.38	5691	30.14	0.005338	1.039
D	0.3648	20.94	3872	20.51	0.005408	1.053
Total	1.7417	100.00	18881	100.00		
Component	Unknown					Adjusted Area %
	Peak	Weight	Normalized			
	Area	(%)	Weight%	Area $\times F$		
A	3862	19.84	19.66	3862	19.66	
B	5841	30.93	30.66	6022	30.66	
C	4926	26.29	26.06	5118	26.06	
D	4406	23.83	23.62	4640	23.62	
Total	19035	100.89	100	19642	100.00	

areas to give the concentration per unit area. One component (A) was chosen as reference and assigned a response factor of 1. The other components' response factors are determined by dividing their concentration per unit area by A's concentration per unit area. The response factors are relatively insensitive to flow and temperatures changes and can be reproduced over long periods of time with this detector. Now the unknown sample can be chromatographed and the areas are measured. Each area is multiplied by the weight percent per unit area to obtain the raw weight percents in the unknown. Due to the difference in sample sizes, the sum of raw weight percents is not necessarily 100%. By normalizing the total weight percent to 100%, the error introduced by sample size difference can be corrected. The same results will be obtained by correcting the peak areas with response factors and use adjusted area percents as weight percents. The major disadvantage of this technique is that all peaks must be standardized to do the normalization, regardless of whether they are of interest to the analyst. It's difficult to be done with real-life samples that may contain

many components, some of which may not be resolved at all.

- Internal standardization also compensates for the difference in sample sizes. Instead of normalizing the total weight percent, an internal standard is used as a reference. Assuming component C is of interest and there is no component A present in the unknown, a known weight of A is added to the unknown as an internal standard. Using the same procedure shown in Table 2.1, response factors can be determined for components A and C. The sample is then chromatographed and the peak areas are measured. Since the relationship holds:

$$F_A/F_C = \frac{W_A}{A_A} / \frac{W_C}{A_C} \quad (2.1)$$

where F_A and F_C are response factors of A and C, W_A and W_C are weights of A and C, and A_A and A_C are areas of A and C, the weight of C in the sample can be calculated:

$$W_C = \frac{A_C}{A_A} \times \frac{F_A}{F_C} \times W_A \quad (2.2)$$

This internal standard method is the most precise method of quantitative analysis by GC. Its advantages are well worthy of the effort for sample preparation.

2.2.2 Calibration Standards

As shown in the previous section, the use of an internal standard is beneficial for both qualitative and quantitative analysis. In order to take full advantages of the internal standard, the WIMS μ GC chose to put a standard vapor source on board. The calibration source will add internal standard vapor into the gas samples, so that both relative retention data and internal standardization can be used for qualitative and quantitative analysis. The on-board calibration source will also help to monitor the μ GC for instrument drifting, aging and malfunction.

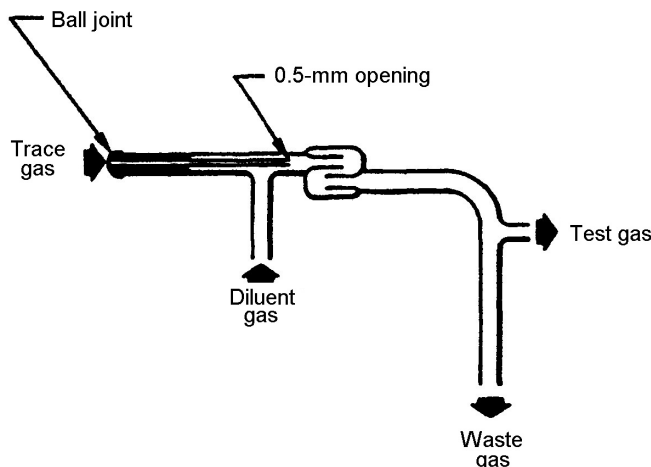


Figure 2.6: Sketch of a system with a low-flow inlet for making single dilutions [10]

For a traditional GC system, the gas standards can be prepared statically or dynamically. Static method involves weighing and mixing gases or vapors in a container. Static standards can be purchased in small pressurized cans or prepared in the lab. Although static standards are being used extensively for calibrating conventional GC, it's not appropriate for the μ GC. First, mixing gases in the field is not practical, while pre-mixed gas standards suffer from problems caused by transportation and storage, such as wall adsorption, reaction and decomposition. Secondly, it is difficult to introduce static standards into gas samples due to the sampling scheme used by the WIMS μ GC.

Dynamic methods involve the mixing of two or more pure gas flows at a constant, known flow rate into the mixing junction. Figure 2.6 shows a mixing system that makes single dilution. Due to the establishment of equilibrium between the adsorption and concentration in the flow stream, the adsorption problems are negligible in the dynamic standard system [10]. Another advantage of the dynamic method is that the concentration can be easily changed in a wide range by adjusting the flow rate of one or more of the gas components. The dynamic method is usually more complicated and expensive. However, by taking advantage of the already built-in vacuum pump,

which can be used to handle the diluent gas flow, the dynamic system will not cause a significant increase in the complexity of the μ GC.

Trace gas flows in the dynamic system can be generated by making use of the saturated vapor pressure (SVP) of a volatile liquid. Mixtures in the percentage range can be easily achieved by passing diluent gas through a thermostatted bubbler [9]. When the diluent gas flows are maintained low enough to ensure saturation, the concentration of the standard can be calculated as [9]:

$$C = \frac{SVP}{total\ pressure} \times 100\% \quad (2.3)$$

The vapor pressure of the output of the bubbler can be adjusted by changing the temperature of the bubbler or changing the total pressure. However, for a vapor concentration in the low parts per million or parts per billion range, diffusion methods or permeation methods should be used instead. Typical configurations of the diffusion tube and the permeation tube are shown in Figure 2.7. Given a constant temperature, constant vapor generation rates can be achieved with either configuration. The generation rate of the diffusion tube may be varied over a wide range by changing the dimension of the diffusion path while the permeation rates can be varied by changing the area and thickness of the polymer wall.

Among all the configurations, the diffusion tube is the one that has the best compatibility with MEMS technology. The bulb part and the capillary tube can be fabricated with established micromachining technologies. In addition, the diffusion tube configuration is capable of generating vapor concentration at low parts per million, which is the range of interest for the μ GC. For those two reasons the diffusion tube configuration was chosen for the on-board calibration source. There is a problem associated with the miniaturization of the diffusion device though. Because of the small distance (<1mm) between the end of the diffusion tube and the surface

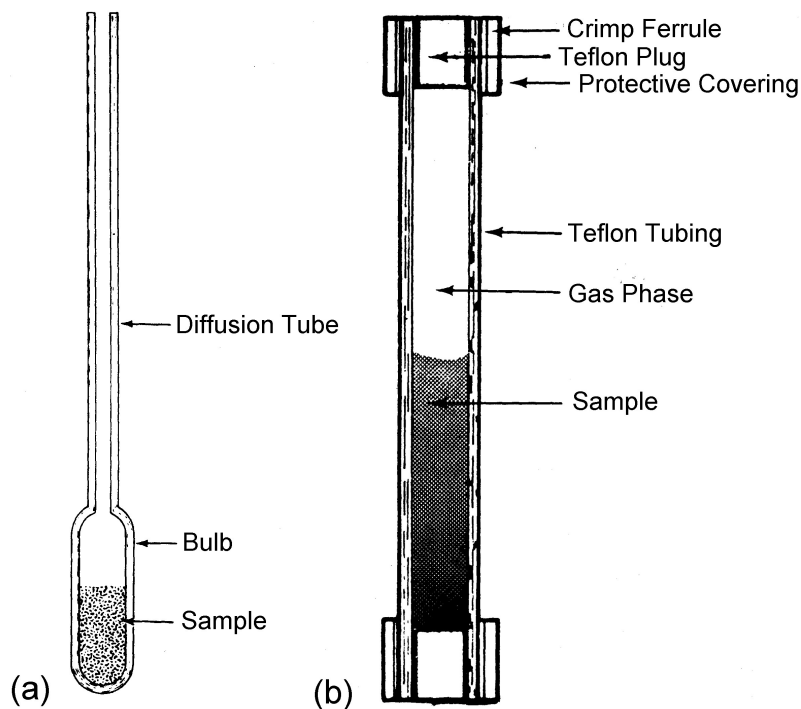


Figure 2.7: Cross-sectional diagram of (a) a diffusion tube, (b) a permeation tube (courtesy of Analytical Instrument Development)

of the volatile liquid in the miniaturized diffusion device, the liquid can get into the diffusion tube and cause malfunctions, when the device is subject to any movement. To solve this problem, porous media are used as an immobilizer to hold the liquid by the capillary force. The detailed design of the calibration source will be discussed in Chapter 5. In order to obtain a stable vapor generation rate over time, there are several requirements for the porous material. First, the porous material needs to have a very uniform pore size and porosity in depth to maintain a constant vapor pressure as the calibrant in the porous media is being depleted. Secondly, the porous material needs to provide good mechanical strength to hold the calibrant liquid and to withstand the capillary forces. Thirdly, the porous material needs to be chemically compatible with the calibrant liquid. A typical volatile liquid used in diffusive calibration vapor source is n-decane. The porous material, therefore, should not show any change in its morphology when it is in contact with n-decane.

2.3 Inlet Filter for the μ GC

The use of ambient air as a carrier gas frees the WIMS μ GC from cylinders of compressed gases. However, it also poses challenges. One of the potential problems caused by this configuration is the entering of particulates and moisture into the μ GC system. Due to the small feature of the micro machined channels and valves, the existence of particles and moisture will dramatically degrade the detection sensitivity and shorten the lifetime of the GC [11]. Therefore, the design of the inlet filter is critical to the success of the environmental testbed.

Filters are usually characterized by their pressure drop, filtration efficiency and filtration capacity [12]. The μ GC is designed to operate with an on-board micro vacuum pump. The limited pumping capacity of the micro pump asks for an inlet filter with very low pressure drop. At the same time, the filter should be effective in removing particles with size down to submicrons. Those two requirements, however, are naturally exclusive. To have a higher filtration efficiency at small particle size usually requires smaller pores in the filter, which will inevitably cause an increase in the pressure drop. To achieve a good balance between these two parameters is the primary challenge for designing a filter. The filtration capacity is critical for the μ GC application. Since it is not practical to replace an integrated filter in the micro system, a small filtration capacity may be the limiting factor for the whole system's lifetime. When the μ GC system is in operation, the particle filter will be exposed to all kinds of solvent vapors. The chemical compatibility, therefore, is also very important for the inlet filter.

Due to the restriction on power consumption, only mechanical filters were considered for this application. The filtration of a mechanical filter is the result of several mechanisms acting together, as shown in Figure 2.8. The most obvious mechanism is straining, where a particle is larger than the opening of the filter structure and cannot pass through. In another method, as gas flows through a filter, it changes direction

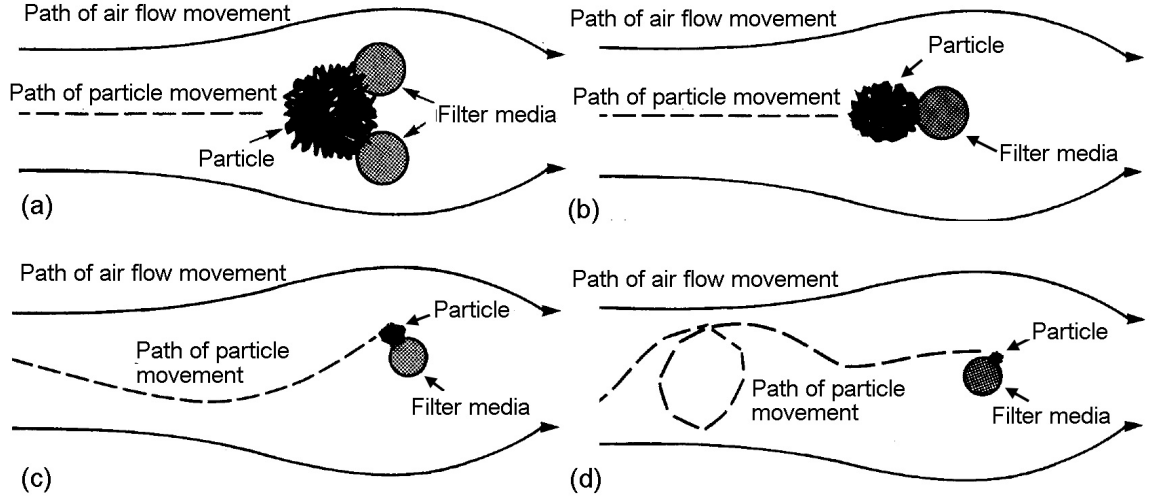


Figure 2.8: Mechanism of filtration: (a) straining, (b) impingement, (c) interception, and (d) diffusion [13].

as it goes around the structure. Heavy particles, however, cannot follow the abrupt changes in direction because of their inertia. As a result, they do not follow the air stream and collide with the filter structure. This mechanism is called impingement. There is a special case of impingement where a particle follows the airstream. But because of its finite size, it is intercepted as it approaches the collecting surface at a distance equal to its radius. The particle then will be retained by adhesive forces between the collecting surface and the particle. One of the adhesive forces is “van der Waals” force. Another principle is known as diffusion. When particles are very small, their directions and velocities are influenced by molecular collisions (called “Brownian movement”). As a result, these particles do not follow the air stream. Instead, they walk across the direction of flow in a random fashion. Their erratic motion causes them to collide with the collecting surface and be retained by the adhesive forces.

Several micromachined filters exist in the literature. Joon et al. fabricated a thin nitride membrane ($1\text{--}3\mu\text{m}$ thick) with perforation that are smaller than the diameters of the targeted particles [14]. The pore size of the reported filter ranges from $1\mu\text{m}$ to $12\mu\text{m}$. Kittilsland et al. presented a filter that consists of two silicon membranes with

holes misaligned. By changing the membrane separation distance, filtration of particle down to 50nm can be achieved [15]. Tu et al. designed and fabricated nanopore filters using sacrificial oxide removal and direct bonding techniques. Removal of particles as small as 44nm has been demonstrated [16]. Those filters, however, are developed for particle sorting and sampling, and are fundamentally not suitable for the inlet application. The main acting filtration mechanism in this type of filters is straining. It functions in an on/off basis, where particles that are bigger than the pore size are trapped while particles that are smaller than the openings will pass through. To remove submicron particles, the pore size has to be submicron or smaller. This is very ineffective with respect to the pressure drop. In addition, particles will be collected only at the surface of the filter, which limits the capacity of the filter.

To achieve a better balance between collection efficiency and pressure drop and to obtain a higher capacity, depth filtration as demonstrated in traditional fibrous filters is more desirable for the inlet filter. Due to the relatively long and tortuous path in the fibrous media, interception and diffusion are more pronounced, which enable the filter to capture particles smaller than the openings in the media. Also, particles will be retained along the full depth of the filter. The capacity of the filters, therefore, are much higher than those of surface loaded ones. Sato et al. demonstrated a microfilter with 3-D micromesh structure in SU8 by multi-angle exposure. Structures with mesh sizes of $57.3\mu\text{m}$, $27.3\mu\text{m}$, and $10.0\mu\text{m}$ have been simultaneously integrated in a microfluidic channel [17, 18]. This device is very promising for a lab-on-chip system. However, the mesh size is still too big for the inlet filter. To effectively remove particles down to sub-micron diameter requires pores with size around or less than $1.5\mu\text{m}$ [19]. The incompatibility of SU8 with the organic vapors, for which the μGC is designed, further excludes the possibility of using this type of filter as the inlet filter for the μGC . Therefore, integrable porous material with smaller openings and better chemical compatibility needs to be developed for the inlet filter. Based

on specifications of commercial filters, a porous membrane with tortuous pores of $1\sim 1.5\mu\text{m}$ diameter and $\sim 100\mu\text{m}$ long will be a good start point [19].

2.4 Porous Silicon Technology

Formation of porous silicon by electrochemical anodization of silicon in an HF based electrolyte was first discovered by Uhler [20] in 1956. Early interest in this material was almost exclusively related to its use for device isolation in integrated circuits [21, 22]. In the early 1990s, the discovery of room temperature photoluminescence from porous silicon by Canham [23] started a renewed interest in this material. Since then, porous silicon has been developed as a means of increasing the functionality of silicon technology. There are now in excess of 400 publications about porous silicon per annum [24]. New types of porous silicon have been added into the family and its applications now span the fields of electronics, optics, optoelectronics, micromachining and biomedical engineering.

2.4.1 Micro-structures

Much of the porous silicon's utility can be credited to its wide range of morphologies. Figure 2.9 illustrates schematically the great variety of morphologies (pore diameter, pore spacing, orientation, etc.) that can be obtained with porous silicon.

The resulting material can vary from nano porous silicon with a fine structure to macro porous silicon with regular macro pore arrays by changing anodization conditions, which include substrate type, crystal orientation, doping concentration, electrolyte composition, current density, temperature, and photo illumination. Each material has its own unique properties and can be used for different applications.

- Nano porous silicon is one of the first discovered types of porous silicon. It's typically made from lightly doped p type material or n type silicon with illumi-

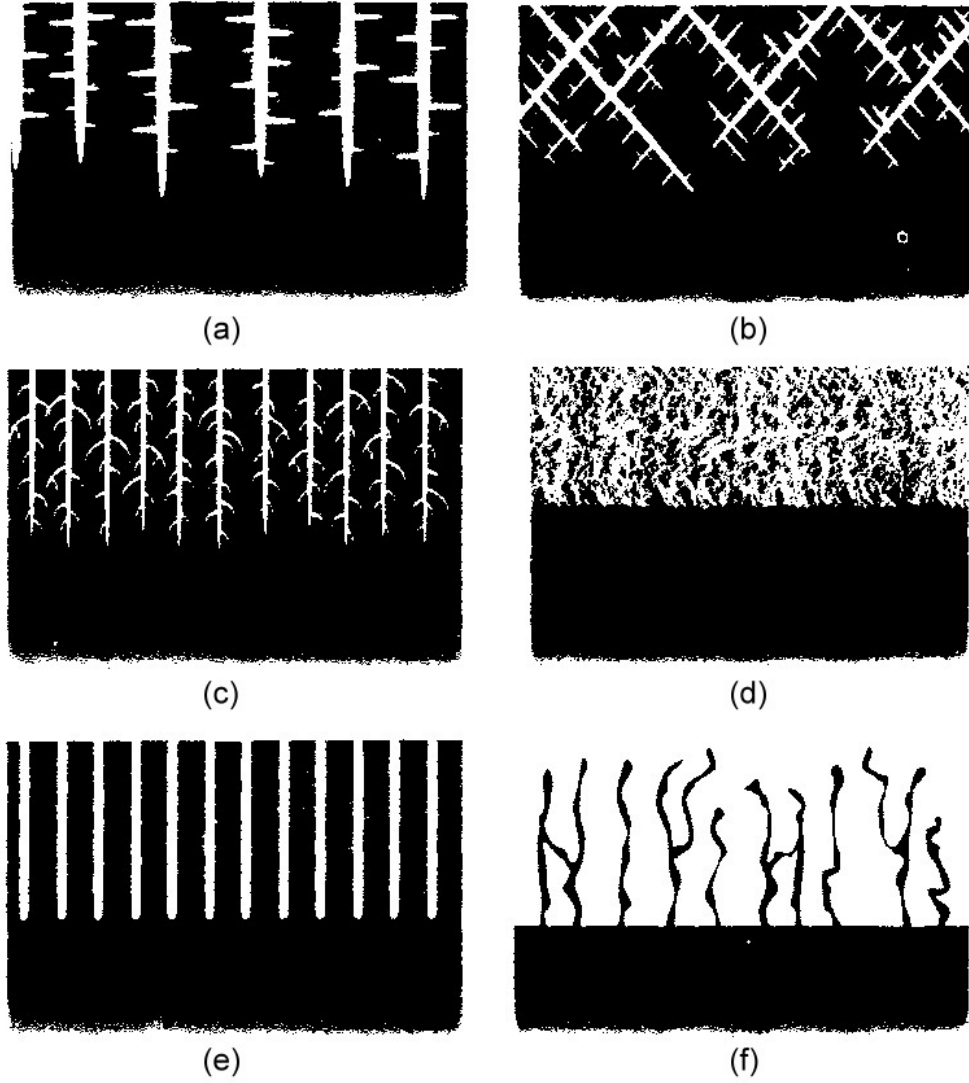


Figure 2.9: Schematic illustration of typical porous Si morphologies. (a) $n^-(100)$ oriented wafer anodized in the dark, (b) $n^-(110)$ oriented wafer, (c) n^+ wafer with dilute aqueous HF, (d) p^- wafer with concentrated aqueous HF (e) $n^-(100)$ oriented wafer with backside illumination, and (f) p^+ wafer with dilute ethanoic HF [24].

nation. Due to the nano scale dimension (a few nm) of its skeleton, quantum size effect becomes predominant [23]. Unlike bulk silicon, this type of porous silicon shows a direct bandgap structure and is extensively studied for its photoluminescence and electroluminescence properties [23–25]. Recently, it is also being studied as sensing materials for gas sensors, humidity sensors and biochips due to its extremely high specific surface area [24, 26–31].

- Meso porous silicon is usually made from heavily doped material. The resulting film has feature size around tens to hundreds of nanometers. Compared to nano porous silicon, it has better mechanical strength and provides better manufacturability. Relatively thick films ($>100\mu\text{m}$) and membrane structures are both possible with meso porous silicon [32, 33]. Due to its large surface area, meso porous silicon can be easily oxidized to provide thermal or electrical insulation. This property has been demonstrated in microhotplates and Full Isolation by Porous Oxidized Silicon (FIPOS) [34, 35]. The large surface area also causes dissolution of meso porous silicon in KOH or TMAH at room temperature. Combined with other features, such as frontside process, planar surface, deep cavity and being CMOS compatible, meso porous silicon makes a good sacrificial material for micromachining [36–38].
- Macro porous silicon is a relatively new material. However, since the discovery of n type macro porous silicon by Lehmann and Föll in 1990 [39], the formation of perfect macro pore array structures have been quickly developed into an art [40, 41]. Arrays of deep trenches with an extremely high aspect ratio have been demonstrated in both n type and p type materials [42, 43]. Pore size and spacing can be accurately controlled from half micron to a few microns [44]. Defects can be purposely introduced [41]. Pore diameter can be modulated in depth. With some new electrolytic solutions and specially prepared substrates

(several degrees off the (100) plane), even slanted pores are possible [45]. One of the early applications of macro porous silicon was to make high density capacitors with its large but well controlled surface area [46]. By coating the walls with enzymes, the large surface of porous silicon also offers possibilities to synthesize specific chemicals in a micro format at chip dimensions [47]. A rather novel use of macropores is in the area of “Brownian motors or pumps” [40]. A membrane of macropores with a saw tooth like cross section was used to separate two reservoirs with particles of two different sizes suspended in carrying liquid. By pumping the liquid back and forth, small and large particles will be separated into different reservoirs. The most unique application of macropores, however, is in the area of photonic band-gap (PBG) materials, so-called photonic crystals [48]. The periodic variations of the index of refraction at a scale that matches the wave length of light in the photonic crystals has the similar effect on the light waves as a real crystal structure does to electron waves. Therefore, an optical band-gap system can be developed, blocking light propagation in certain energy regions. Macropore arrays can serve as an optical filter along the pore direction as well. Photons with wavelength smaller than the pore diameter pass through, others are blocked. A filter for passing short wave lengths has been described and produced by Lehmann et al. [49]. Macro porous silicon also has been used in micromachining. Deep three dimensional structures have been demonstrated on a macropore array substrate with “Ottow” process [50]. A promising method for fabrication of lead collimators for x-ray imaging has been reported by Lehmann [51]. A macropore array was used as a mold and sacrificial material to produce a lead grid.

2.4.2 Manufacturability

In addition to its versatility in morphologies, porous silicon also provides some unique properties to facilitate the fabrication process. Figure 2.10 shows the typical current-voltage ($i-v$) characteristics for different silicon substrates [52]. The doping dependency of the $i-v$ characteristics can be used for the selective formation of porous silicon. For example, a potential close to zero will give rise to a current density of $40\text{mA}/\text{cm}^2$ in a heavily doped p type region, while no current will be generated in a lightly doped n type region. Therefore, if those two regions are put adjacent to each other, porous silicon will be preferentially formed in the heavily doped p type region. According to Figure 2.10, n^+/n^- , p^+/n^- and p/n pairs all provide good selectivity. Utilizing the well established impurity doping technologies for silicon, both the lateral dimension and the thickness of porous silicon can be accurately controlled [53, 54]. Unlike KOH or EDP etching that stops at heavily doped regions, porous silicon etch-

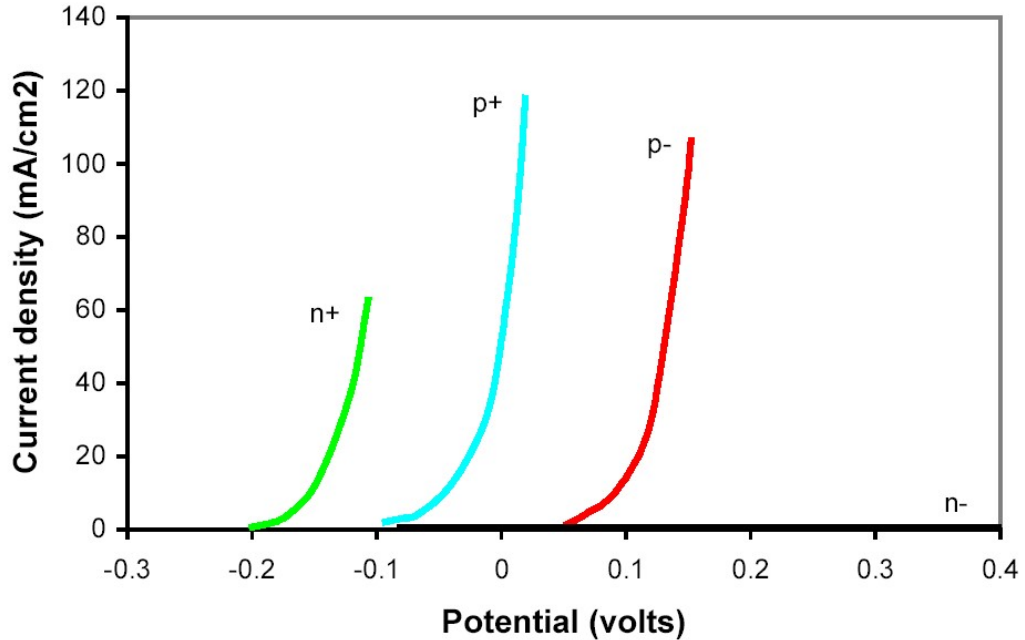


Figure 2.10: Comparison of the anodic current-voltage characteristics obtained from p and n type silicon in a 35% HF solution and different doping levels (n^+ and p^+ : 10^{19}cm^{-3} , n^- and p^- : 10^{15}cm^{-3}) [52].

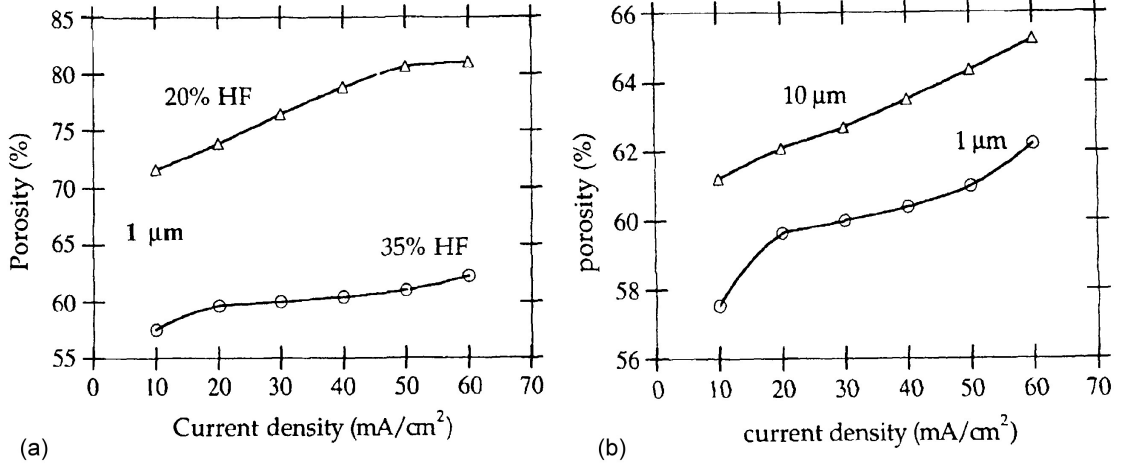


Figure 2.11: (a) Porosity as a function of current density for two different HF concentrations with p substrate ($\sim 1\Omega\cdot\text{cm}$); thickness of the porous layer = $1\mu\text{m}$. (b) Porosity as a function of current density for two different thicknesses (1 and $10\mu\text{m}$) with p substrate ($\sim 1\Omega\cdot\text{cm}$); HF concentration = 35% [52].

ing leaves lightly doped regions intact. This would allow the fabrication of CMOS circuitry in an etch-stopped region. MEMS devices can be built adjacent to the CMOS circuitry using porous silicon as sacrificial material.

Not only can the formation region of porous silicon be specifically defined, the pore size and porosity of the resulted film can be controlled as well. As shown in Figure 2.9, the type of porous silicon, nano, meso or macro pore, that is being produced is mostly determined by the choice of substrate type and electrolyte. Fine tuning of the pore size and porosity, however, can be achieved by changing the etching current density within certain limits. Typically, higher current density leads to larger pores and higher porosity, as shown in Figure 2.11 [52]. The already formed porous silicon structure, however, is not affected by further change in the etching current density [55]. This passivation mechanism is explained in several existing models by the depletion of holes, which are necessary for etching, in the formed silicon skeleton. Consequently, the remaining porous structure can not be further anodized [56]. Since the current density can be easily modulated during the etching, the direct correlation between the porosity and current density makes it possible to form a stack of porous

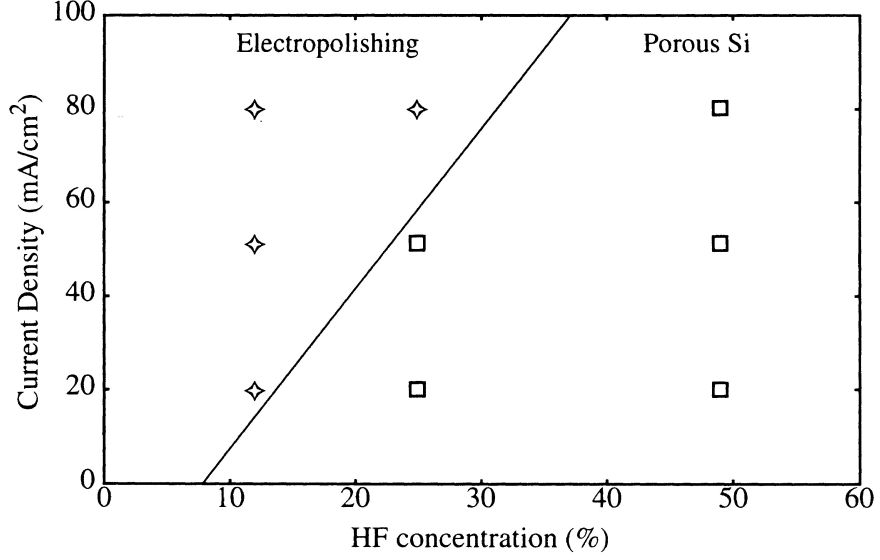


Figure 2.12: Measured electropolishing boundary for lightly doped p^- type silicon as a function of HF concentration and current density [58].

silicon layers with different porosity in depth. Those periodic structures have been used as interference filters or mirrors for visible red and infrared regions of the electromagnetic spectrum [57]. Increasing the current density beyond a critical value will result in electropolishing, which generates a very smooth surface instead of pores [52]. The electropolishing boundary for p^- silicon, roughly calculated from the different combinations of etching parameters used, is plotted in Figure 2.12. Electropolishing is also selective with respect to dopant concentration. This property has been used for releasing micro probes from the silicon substrates by electropolishing away buried p^{++} or n^{++} regions [58]. The same passivation mechanism that works for pore formation applies to the electropolishing as well. By alternating the etching current density between electropolishing regime and pore formation regime several times, interesting structures like multi-walled microchannels can be formed [59]. A very elegant way of using porous silicon technology has been demonstrated by Lammel et al. in a tunable optical filter [60]. The Bragg mirror or Fabry-Pérot bandpass filter plate for transmission wavelengths between 400nm and $8\mu\text{m}$ at normal incidence has the periodic

structure consisting of layers of varying porosity, created by porosity modulation. A pair of Ni/nitride heaters are connected to the side of the filter plate. In the same etching process, porous silicon is also formed underneath the heater, except the anchor area. The porous silicon is then detached from the substrate by sub-surface electropolishing, leaving the filter plate suspended by arms made from the Ni heater, silicon nitride and porous silicon. The arm also serves as a thermal trimorph actuator. By flowing current through the Ni heater, the tilting angle of the filter plate can be adjusted.

In spite of its porous structure, porous silicon is still a single crystalline material and silicon epitaxial layers with good quality can grow on the top of it. This fascinating property gives rise to a new way to fabricate single crystalline MEMS structures. First, porous silicon can be locally formed. Then epi layers can be deposited and patterned. After removing the underlying porous silicon in room temperature KOH or TMAH, the structure made from the epi layer will be released. This method has very good process control, since the lateral dimension of the porous silicon region and the thickness of the epi layer can be well defined. In addition, because it does not require backside lithography, bonding, or expensive SOI substrates, the process is simple and cost effective.

One of the most famous applications of porous silicon is in the field of SOI wafer technology. New SOI wafers named ELTRAN[®] (Epitaxial Layer TRANSfer) have been developed by Canon Inc. The process flow is shown in Figure 2.13. double layered porous silicon is first formed on a silicon wafer (seed wafer) by current density modulation. The top layer has low porosity and serves as a seed layer for epi growth. The bottom layer has high porosity and serves as a “zipper”, which will be explained later. After growing epitaxial silicon and silicon oxide on the top of the porous silicon, the seed wafer is bonded to a handle wafer. The bonded wafer pair is then “unzipped” along the high porosity porous silicon layer, transferring the silicon dioxide and epi

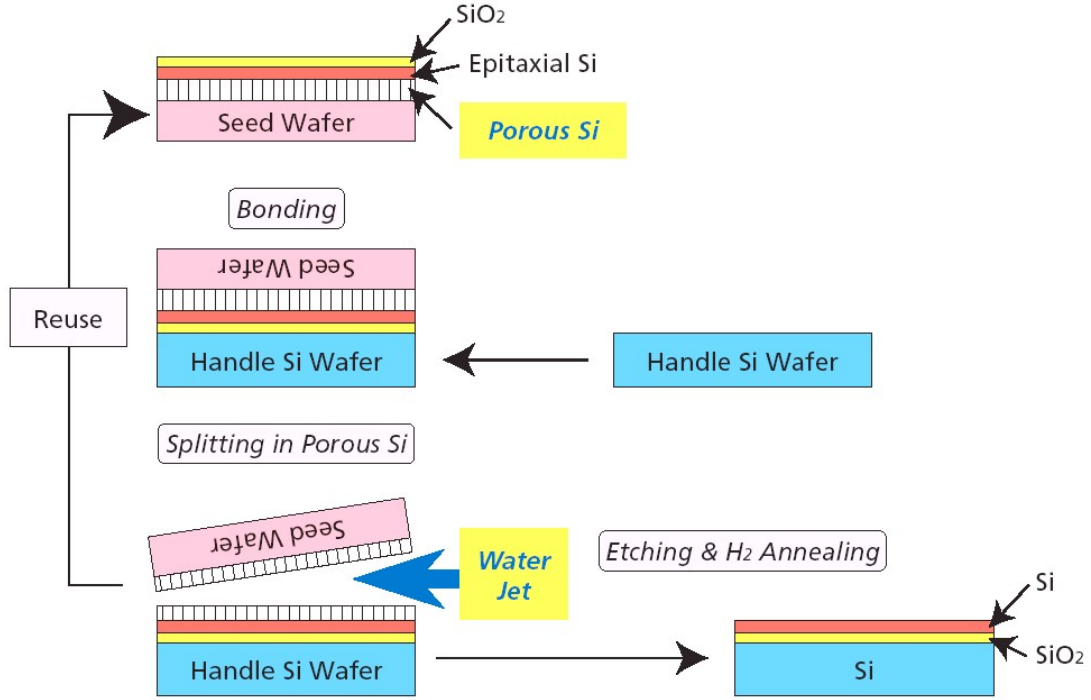


Figure 2.13: ELTRAN® process flow [61]

silicon layers to the handle wafer. The surface of the handle wafer is then etched and annealed to produce high quality SOI wafer. The seed wafer, in the meanwhile, can be reused [61].

This list of porous silicon's properties and their corresponding applications is by no means complete. However, it's safe to conclude that porous silicon is a very versatile material with great potential for many new applications. The researchers of this project chose to investigate porous silicon as the porous material for the calibration source and the inlet filter. This is due to its excellent manufacturability and integrability with micro systems. Since porous silicon is made from a silicon substrate, porous silicon technology can make use of the well established silicon technology for micro-manufacturing. Device integration and packaging of porous silicon can also benefit from bonding processes that are readily available for silicon substrates. With the great variety of morphologies and the tunable pore size and porosity, porous silicon is a very promising porous material for micro systems.

Chapter 3

Development of Porous Silicon Materials

The most important part of this research is to produce and optimize porous silicon materials for each device. For the calibration source, a very thick porous layer with uniform pore size in depth is required to obtain stable vapor evaporation. The inlet filter, on the other hand, needs a thick porous membrane with a tortuous pore path. Based on the information about pore size, pore morphology, and mechanical strength of the resulting material, meso PS and macro PS were chosen as the candidates for the two devices.

3.1 Formation Mechanisms

In order to produce and optimize porous silicon materials for each application, it is important to understand the fundamentals of porous silicon formation. The most common method of forming porous silicon is electrochemical dissolution of silicon in a hydrofluoric acid (HF) based electrolyte. In the dissolution process, a silicon wafer serves as the anode, while any HF resistant conducting material, such as Pt, is used as the cathode. For this reason, the dissolution process is often called anodization. Figure 3.1 shows the typical J - V curve of p^+ -Si in dilute aqueous HF solution [24]. In general, anodization under galvanostatic conditions is preferable to achieve a good reproducibility. Pore formation is obtainable for $J < J_{PS}$. If the applied current density is larger than J_{PS} , electropolishing will occur, which generates a very smooth

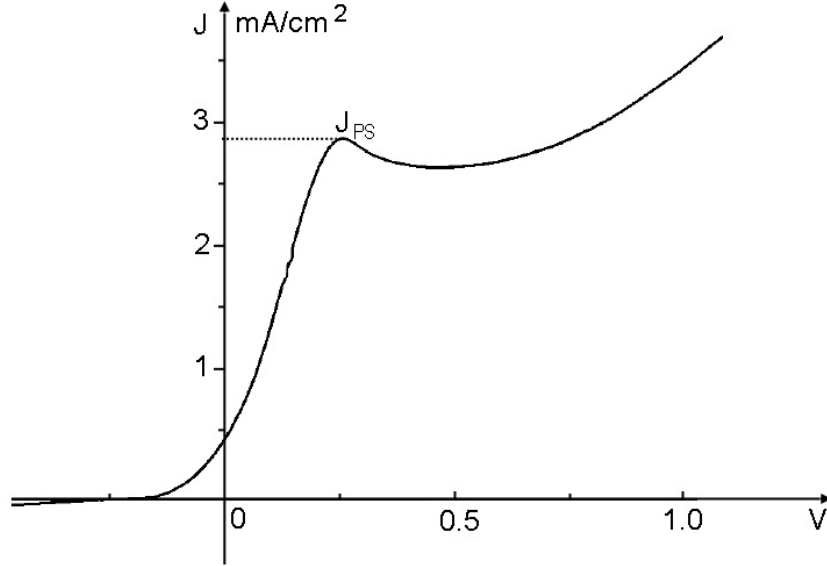


Figure 3.1: Typical J - V curve of p^+ -Si in dilute aqueous HF solution. Pore formation is obtainable for $J < J_{PS}$ [62].

surface.

A number of models have been proposed to explain the formation of porous silicon. Although the exact mechanism is still uncertain, it is generally agreed that electronic holes (h^+) have to be available at the Si-HF interface [56,63]. If holes are present in a certain surface area, dissolution of the silicon will occur there, which causes pores to propagate. Similarly, a surface area that is depleted of holes will be passivated, which forms the walls. Hole depletion will only occur if any hole that reaches the interface is immediately consumed in the dissolution reaction. This requires that the chemical reaction is not limited by mass transfer in the electrolyte. This condition is fulfilled if the current density is below the critical value J_{PS} . For current densities above J_{PS} , the reaction is limited by the diffusion of the fluorine ions. Any outgrowth on the surface will be preferentially etched since they will be reached by fluorine ions first, resulting in a smooth surface. This is the case for electropolishing [64]. For current densities below J_{PS} , the etching is limited by the diffusion of holes. The resulting morphology is then decided by the combined effect of chemical reactions at

the interface and the transport of charge carriers across the interface, which controls the consumption of holes and supply of holes respectively [65].

Details of the chemical reactions of pore formation are not fully understood yet. Several theories suggest that two types of dissolution processes may be involved [44, 66, 67]. The first one is direct dissolution, where the presence of holes weakens Si-Si backbonds and Si-H surface bonds, allowing them to be attacked by negative F^- ions in the HF solution. A compound (SiF_4) is then formed at the surface and breaks away from the substrate. In this reaction path, 1,2,3, or 4 holes may be involved. In the other dissolution process, the anodically biased silicon surface is first oxidized. The silicon dioxide is then dissolved by HF. This reaction path requires four holes [68]. Since in the overall reaction the valence, the number of consumed holes for each dissolved silicon atom, is around 2.7, it is believed that the two dissolution processes must coexist. The actual occurrence percentage of each process is self-adjusting, decided by the anodization conditions. Since the direct dissolution path etches silicon anisotropically while the oxidation path is more isotropic, any shift of the balance between two processes may cause change in morphologies of the resulting porous silicon [69, 70].

The charge transfer characteristic of the Si-HF interface is very similar to that of a Schottky contact [71]. As shown in Figure 3.2, a surface layer that is depleted of mobile charges (Space Charge Region - SCR) forms in silicon when it is in contact with an electrolytic solution [65]. In order to supply holes for the dissolution, a charge exchange must take place across the depletion layer. For heavily doped p or n -type silicon, doping density in excess of $10^{18}cm^{-3}$, the depletion layer is very thin under anodic bias. In this case, the charge transfer is dominated by tunneling at room temperature. The required bias for tunneling, however, is dependent on the pores' curvature. Smaller pore size corresponds to a lower tunneling bias [72]. Therefore the pore size is limited by the maximum radius that allows tunneling, which is around

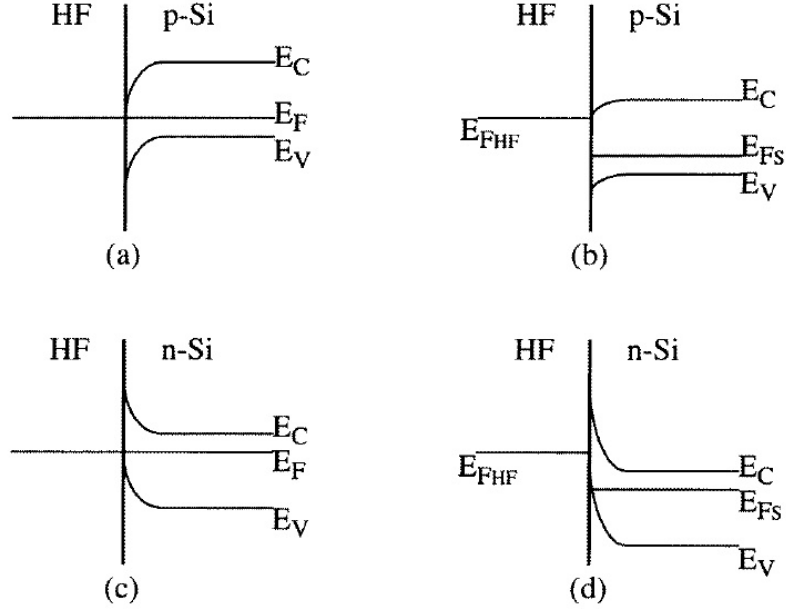


Figure 3.2: Energy band models for the Si–HF interface, which behaves as a Schottky contact. (a) *p*-type silicon at zero bias, (b) *p*-type silicon at anodic bias, (c) *n*-type silicon at zero bias, (d) *n*-type silicon at anodic bias [38]

several tens of nanometer. As the distance between two pores is less than two times the SCR width, this region is fully depleted and therefore passivated. Otherwise, side pores will grow and penetrate the region. This mechanism defines the wall thickness, which is around 10nm. Consequently, mesoporous layers of significant porosity are formed.

In lightly doped *n*-type silicon, where the depleted layer is very thick (several μm), holes may be generated by breaking down the SCR with a very strong electrical field ($3 \times 10^5 \text{V/cm}$). To produce that high electric field, very fine pore tips (10–100 nm) are required to focus the electric field. The wall thickness, which is still defined by the two times the SCR width, however is much thicker compared to the heavily doped material. Consequently, porous layers with low porosity and strongly branched, needle-shaped channels are formed [73].

Holes can also be generated in lightly doped *n*-type silicon by illumination. If the backside of the silicon sample is illuminated, the holes produced by light have to

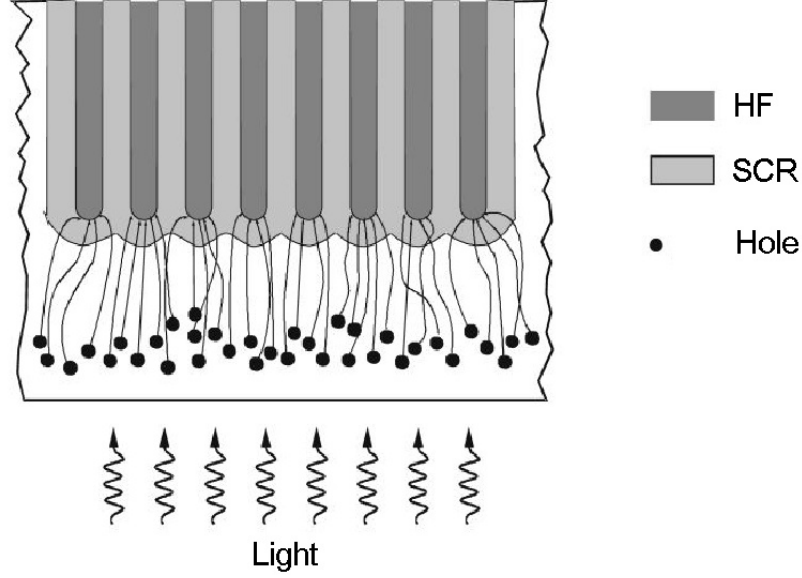


Figure 3.3: Schematic of the diffusion and collection of holes during the anodization of n -type silicon with backside illumination [74]

diffuse through the thickness of the sample to reach the etching interface. However, most of the holes will be collected by the tip of the pores due to the focusing of the electric field lines at the concave surface, as shown in Figure 3.3. The regions between pores, therefore, are depleted and practically passivated. Consequently, macropores with constant diameters and considerable depths are formed [73]. If lithographically defined nucleation is provided, macropore arrays with uniform pore size can be obtained. Lehmann believes that for the case of stable pore growth, the local current density J_{tip} at the pore tip should equal to the critical current density J_{PS} , so that ionic transfer and charge supply are in a steady state condition [64]. Based on this assumption Lehmann proposed a simple formula to calculate the pore diameter d as

$$d^2 \approx A_p = A_{cell} \frac{J}{J_{tip}} = a^2 \frac{J}{J_{tip}} \quad (3.1)$$

where A_p is the pore cross-sectional area, A_{cell} is the area of a unit cell of the pore lattice, a is the lattice constant of the pore array, and J is the overall current density.

By replacing J_{tip} with J_{PS} , d is obtained as

$$d \approx a \sqrt{\frac{J}{J_{PS}}} \quad (3.2)$$

The Lehmann's formula has been successfully demonstrated in producing macro pores with various pore diameter and modulating pore size during the etching process [44].

For lightly doped p -type silicon, the depleted layer is very thin or does not exist at all when the substrate is under anodic bias. The charge transfer is then dominated by thermionic emission at room temperature. A depletion of holes, however, can still occur when the dimensions of a semiconductor particle, wire or sheet is below the Bohr radius of an exciton (a few nm). In this case, holes are depleted independently of the doping density of the substrate due to quantum confinement [56]. Consequently, micropores with pore size around several nanometers and extremely high porosity are formed.

The most puzzling case is the macropore formed in lightly dope p -type silicon. It cannot be fully explained by the depletion of holes. Several theories, such as surfactant coating, hydrogen coating and diffusion instability, have been proposed to explain the passivation mechanism. However, none of them have been well accepted, leaving the formation mechanism of p -type macropores a highly controversial topic.

3.2 Anodization Setup

There are two types of anodization cells that are commonly used to produce porous silicon [24]. Schematic diagrams for both etching cells are shown in Figure 3.4. In the single-tank cell, a metallic contact is made to the backside of the wafer. An O-ring is used to seal around the edge of the wafer so that only the front side of the sample is exposed to the electrolyte. Due to its simple configuration, single-tank cell is the most commonly used arrangement. The double-tank cell, however, uses an electrolytic

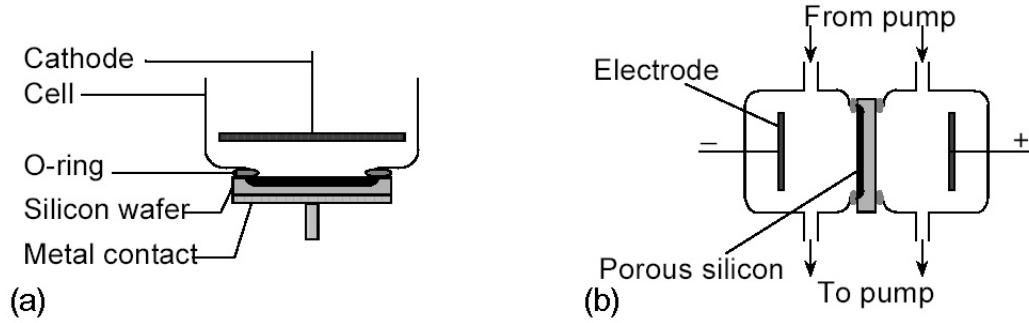


Figure 3.4: Schematic diagram of two types of etching cells, (a) single-tank cell, and (b) double-tank cell [24].

backside contact. It consists of two half cells and the silicon wafer is used to isolate the two half cells. The front side of the wafer serves as a secondary anode in one half cell while the backside of the wafer serves as a secondary cathode in the other half cell. Electrolyte is used for both anodization at the frontside and electrical contact at the backside. Compared to the single-tank cell, double-tank cells can provide better uniformity. It also can handle through wafer etching or alternating frontside and backside etching. Since no metallization of the backside is required, it reduces the risk of metallic contamination. With an HF-resistant window, such as sapphire, both frontside and backside illumination can be applied with the double-tank cell. However, setting up a double-tank cell is more expensive and complicated.

Methods for anodizing silicon have been developed at Michigan Technological University. In order to facilitate different types etching configurations, several etching cells have been designed and machined in house. All of the etching cells are made of HF resistant materials, such as Teflon and polypropylene. Since HF is a very dangerous and aggressive chemical, safety has been given highest priority in the designs of all etching cells. Figure 3.5 shows a single-tank Teflon holder with Pt electrode for etching small samples. The schematic diagram for assembling and using this fixture is shown in Figure 3.6. The cover piece and the bottom piece of the holder are bolted together during the etching process to hold a silicon sample in place. Two viton O-



Figure 3.5: Fixture designed for anodically etching small samples

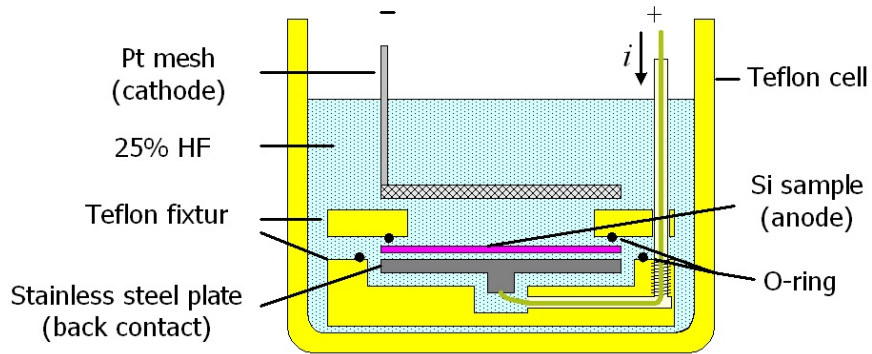


Figure 3.6: Schematic diagram for assembling the small sample fixture

rings seal the cavity behind the silicon sample from any etching solution. The silicon sample sits on a stainless steel plate, which forms the backside electrical contact. A Teflon tube provides a protected access to the backside contact for a wire. Once the fixture is assembled, it is immersed in a tank of HF and anodic etching is initiated by passing current between the backside wafer contact and the Pt electrode. Compared to the setup shown in Figure 3.4(a), this fixture is easier and safer to operate. A single-tank fixture with similar design has been fabricated for 4-inch wafers as well.

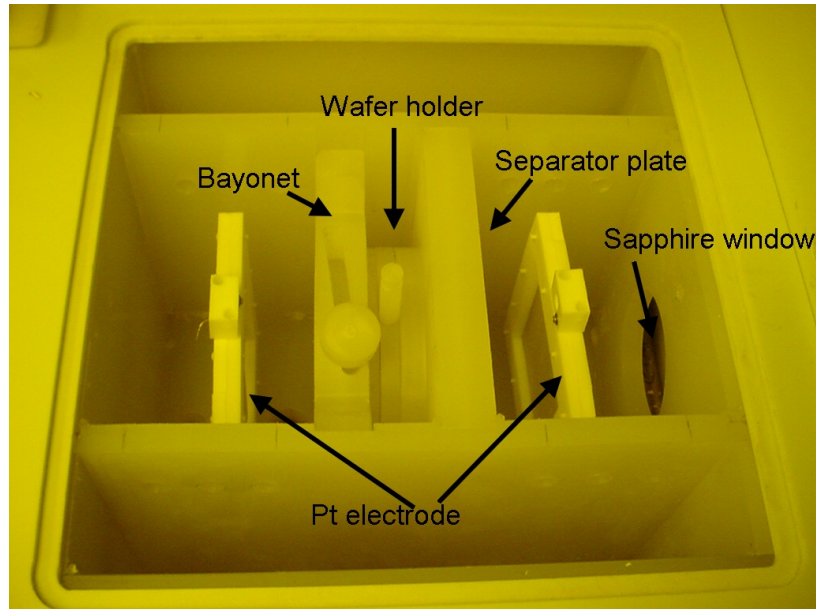


Figure 3.7: A double-tank etching cell for 4-inch wafers

Figure 3.7 shows a double-tank etching cell for 4-inch wafers. It consists of two etching chambers separated by a bayonet locking system. Each chamber has a Pt net mounted on a Teflon frame to serve as the electrode. A silicon wafer is mounted in a wafer holder. The wafer holder is then inserted in the gap between the bayonet and the separator plate. By turning the handle on the bayonet, the wafer holder is pressed against the separator plate. O-rings at the inside and outside surfaces of the wafer holder provide sealing to separate the two chambers. The bayonet locking system provides an easy way to mount the silicon wafer and to remove it from the etching cell and thereby minimizes the handling of the etching solution. This etching cell is also featured with a sapphire window, which will allow the illumination of the silicon wafer during the anodization.

Etching current is provided by a Keithley current source (model 220). The potential drop across the two electrodes is monitored by an HP multimeter (model 3478A). In order to obtain an automated etching process, a Labview program has been developed to control the instruments through a computer. Figure 3.8 shows the interface of the program. The program will read current profile from a file, adjust the output

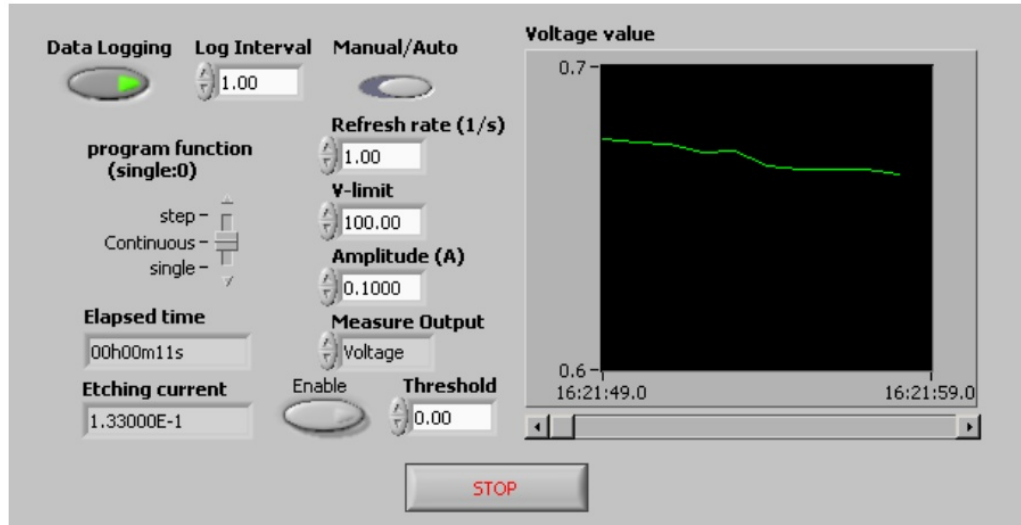


Figure 3.8: The interface of a Labview program for controlling the etching process and recording data

of the current source accordingly, read the voltage values from the multimeter, write them into a file for analysis and turn off the current source when the desired etching time has been reached. Those features are very useful for long duration etchings or etchings with a complicated current profile.

In order to achieve uniform porous silicon formation, two things need to be noted. First, the electrolyte concentration needs to be homogeneous. Decreases in the local concentration of active species may occur as a result of insufficient ionic diffusion or bubble trapping at the etching front. Circulating the electrolyte will help replenish the reactant and removing big bubbles. A circulation system has been installed for the wafer scale etching cell at MTU, as shown in Figure 3.9. The two valves allow the front chamber and backside chamber to be circulated individually or at the same time. Circulation of electrolyte for small samples is achieved with a small peristaltic pump. The wettability of the etching surface also affects the generation and stiction of bubbles. To effectively remove bubbles and allow full infiltration of electrolyte into the pores, a surfactant agent can be added to the HF solution. A few drops of commercially available wetting agents, such as Wacker's NC1001, is sufficient.

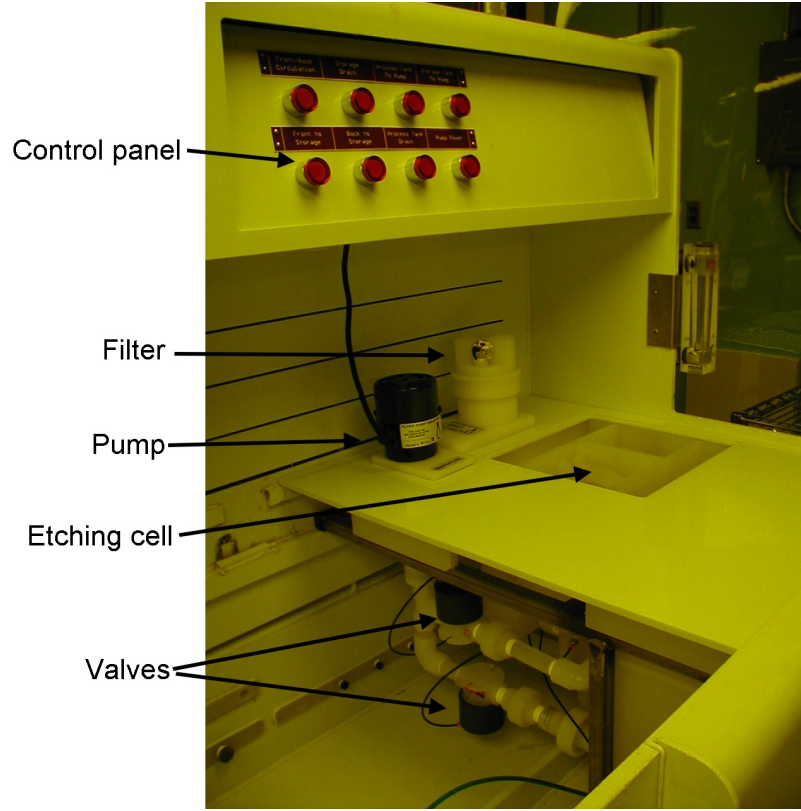


Figure 3.9: A 4-inch etching cell equipped with a circulation system at MTU

Another common practice is to use ethanoic HF solution. Ethanol can reduce the bubble size, eliminate bubble stiction, and thereby improve the uniformity of the porous layer [24]. The second thing that needs to be noted is the homogeneity of etching current density. When the Pt electrodes are big enough, the current density distribution is mostly determined by the silicon sample. For a silicon wafer with low resistivity (typically $< \text{few m}\Omega/\text{cm}$), a good uniformity is obtained without any special treatment. However, for highly resistive wafers (typically $> \text{few m}\Omega/\text{cm}$) a high-dose implantation ($\sim 10^{15}\text{cm}^{-2}$ at 80KeV) of boron for p^- or phosphorus for n^- on the backside is required. The implantation is followed by a rapid thermal annealing (RTA) at 1000°C for 1 minute to activate the dopants. If a metallic backside contact is being used, a metal layer (Al or Cr) needs to be deposited on the backside, followed by a one minute RTA annealing at 550°C . Under these conditions, porous silicon layers with good uniformity can be obtained. It is more challenging to achieve a uniform

current density with patterned wafers due to the current crowding effect. Although the nonuniformity cannot be totally eliminated, it can be reduced to an acceptable level by evenly distributing the porous silicon regions in the mask plate.

3.3 Meso Porous Silicon

Meso porous silicon is one of the candidates that has been considered for the calibration source and the inlet filter. It is also the first type of porous silicon that has been produced at MTU. Figure 3.10 shows the cross section of the first meso porous silicon sample produced by the single-tank etching cell. The substrate is heavily doped ($0.001\text{-}0.002\Omega\text{cm}$) (100) *p*-type silicon. The sample has been etched in 25% HF (50% HF: ethanol = 1:1) at $77\text{mA}/\text{cm}^2$ for 10 minutes.

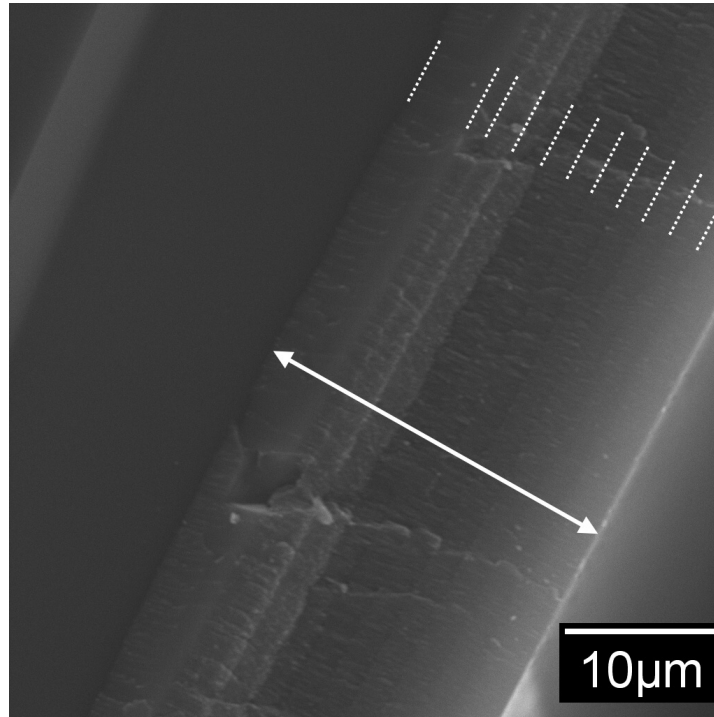


Figure 3.10: SEM photograph showing the meso porous silicon formed by anodically etching heavily doped ($0.001\text{-}0.002\Omega\text{cm}$) (100) *p*-type silicon in 25% ethanoic HF ($77\text{mA}/\text{cm}^2$, 10min). The resulting material consists of several porous layers with different porosities.

3.3.1 *p*-type Meso Porous Silicon

Various anodizations with different current densities and etch time have been performed on the heavily doped *p*-type samples in 25% HF solution to study the etching process. The resulting materials have been characterized by the microstructure, the porosity, and the etch rate. The typical microstructure of the resulting meso porous silicon is shown in Figure 3.11. Consistent with the results reported in literature, the majority of pores propagate along the $\langle 100 \rangle$ direction with smaller pores branching off on the side. As shown in Figure 3.11(b), the average pore size is around 20~30nm. A small portion of porous silicon layer was scraped off the sample and studied in a transmission electron microscope. The electron diffraction pattern in Figure 3.12 proves that meso porous silicon is still a crystalline material.

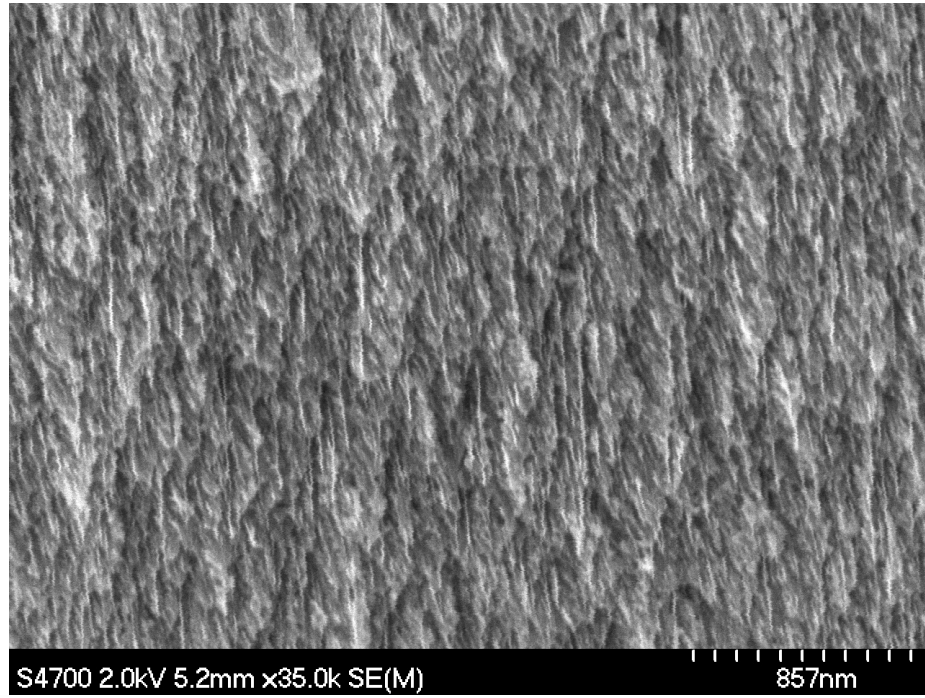
The thickness and the porosity of the porous layer can be determined by gravimetric measurements. The porosity (P) is given simply by the following equation:

$$P(\%) = \frac{m_1 - m_2}{m_1 - m_3} \quad (3.3)$$

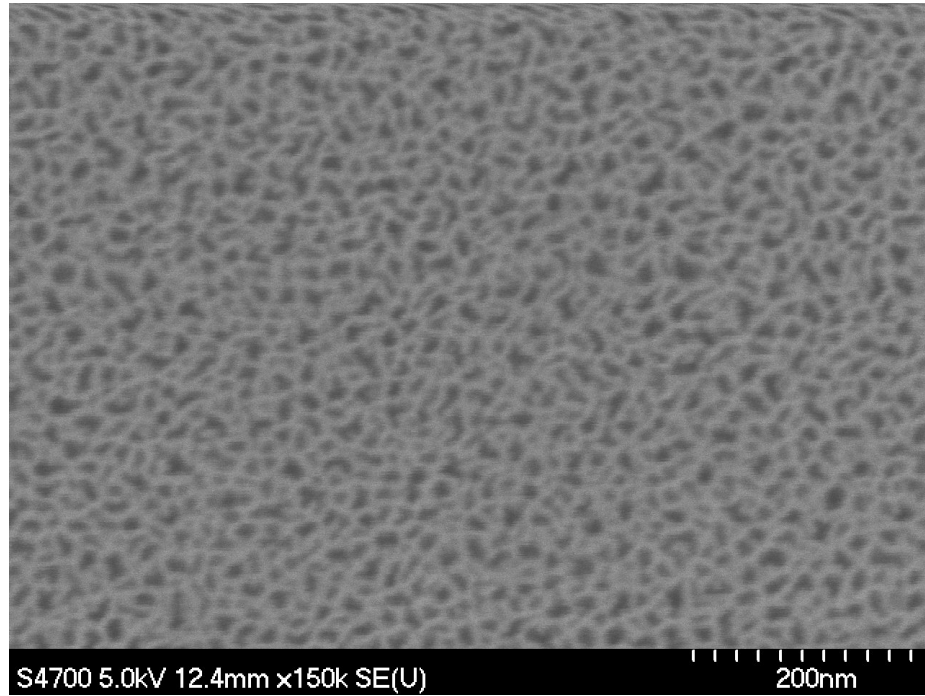
where m_1 is the sample mass before anodization, m_2 is the sample mass just after anodization, and m_3 is the sample mass after dissolution of the whole porous layer in 10% room temperature KOH. With these measured masses, the thickness (d) of the porous layer can be calculated as well:

$$d = \frac{m_1 - m_3}{A \times \rho} \quad (3.4)$$

where A is the area of the porous region and ρ is the density of bulk silicon. The porous layer thickness can also be directly determined by scanning electron microscopy (SEM). The measured porosity and thickness are plotted in Figure 3.13 (a) and (b) as functions of anodization time and as functions of current density. It



(a)



(b)

Figure 3.11: High magnification SEM photographs showing (a) cross sectional view and (b) top view of meso porous silicon layer formed in heavily doped ($0.001\text{--}0.002\Omega\text{cm}$) (100) *p*-type silicon in 25% ethanoic HF ($100\text{mA}/\text{cm}^2$, 300min)

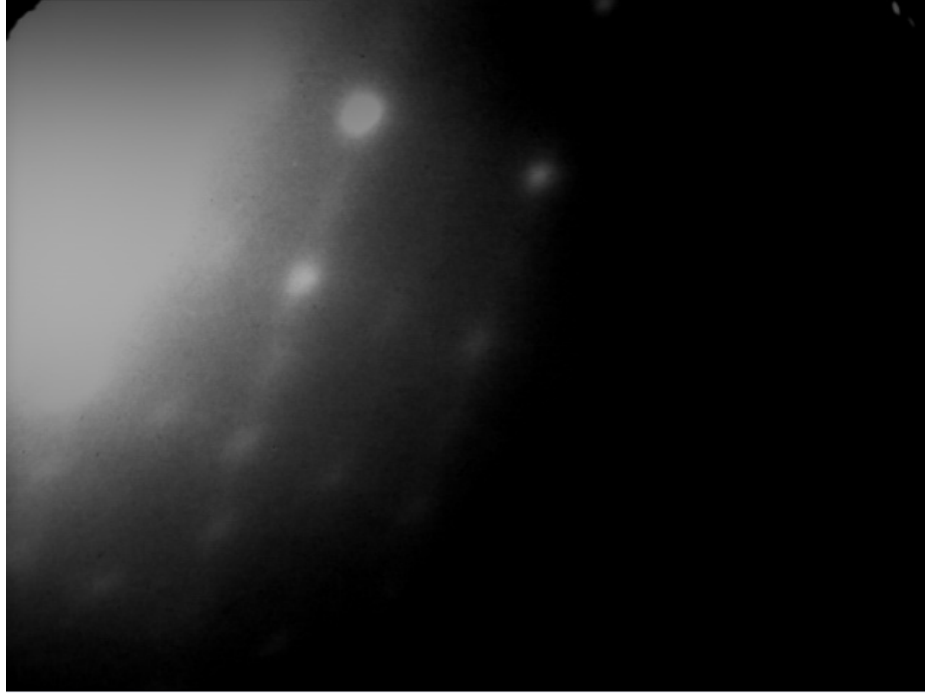
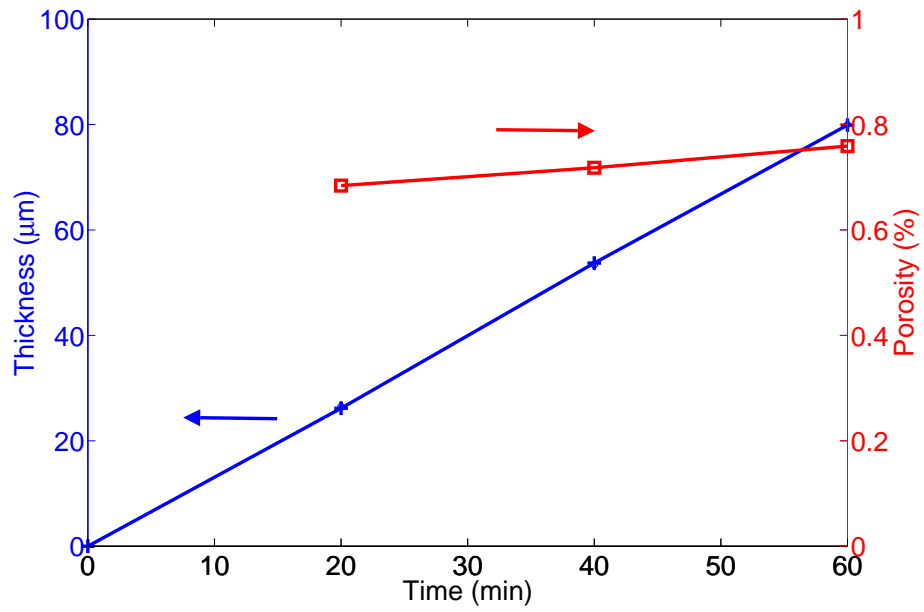
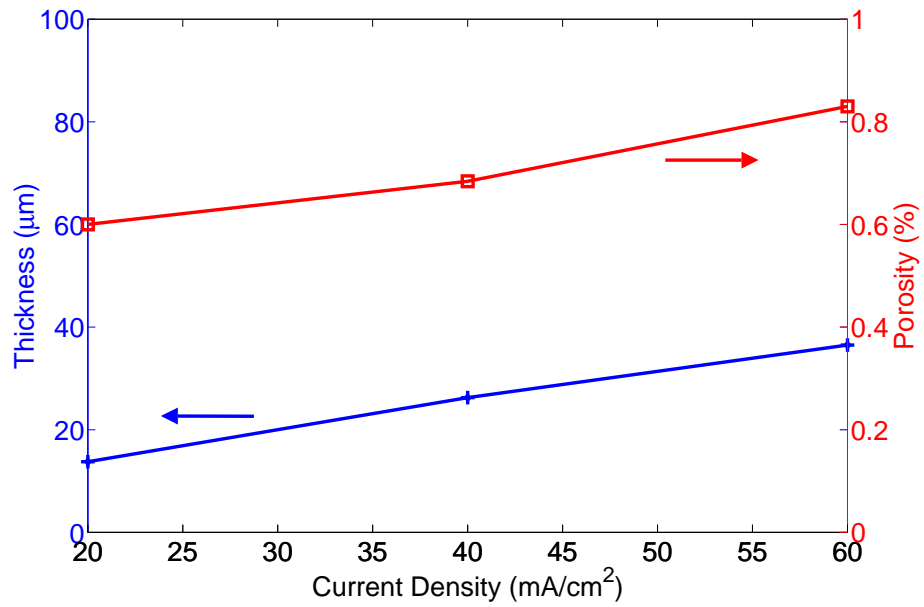


Figure 3.12: Transmission electron diffraction pattern of meso porous silicon showing single crystal diffraction spots

appears that for a given current density, the thickness of the porous layer increases linearly with the anodization time, which results in a constant etch rate. For the conditions shown in Figure 3.13(a), the etch rate is about $1.3\mu\text{m}/\text{min}$. The porosity, however, shows a slight increase as the anodization time increases. This is caused by pure chemical (non-electrochemical) dissolution of the porous layer in the HF. The longer anodization time corresponds to a larger amount of silicon mass chemically dissolved in HF. For a fixed anodization time, the PS thickness increases linearly with the current density, as shown in Figure 3.13(b). This suggests that the anodization rate increases with the current density linearly. For thick PS layer formation, a high etch rate is usually desired to reduce the etching time. However, the resulting porosity also increases monotonically with the current density, as shown in Figure 3.13(b). For most MEMS applications, it is essential for the porous material to have a good mechanical strength. Too high porosity will result in a very fragile structure and cause difficulties in post-anodization processes. Therefore a current density around



(a)



(b)

Figure 3.13: Porosity and thickness of meso porous silicon formed in heavily doped ($0.001\text{-}0.002\Omega\text{cm}$) (100) *p*-type silicon with 25% ethanoic HF as functions of (a) etching time (at $40\text{mA}/\text{cm}^2$) and (b) current density (for 20min).

50mA/cm² is recommended for a good balance between the mechanical strength and the etch rate.

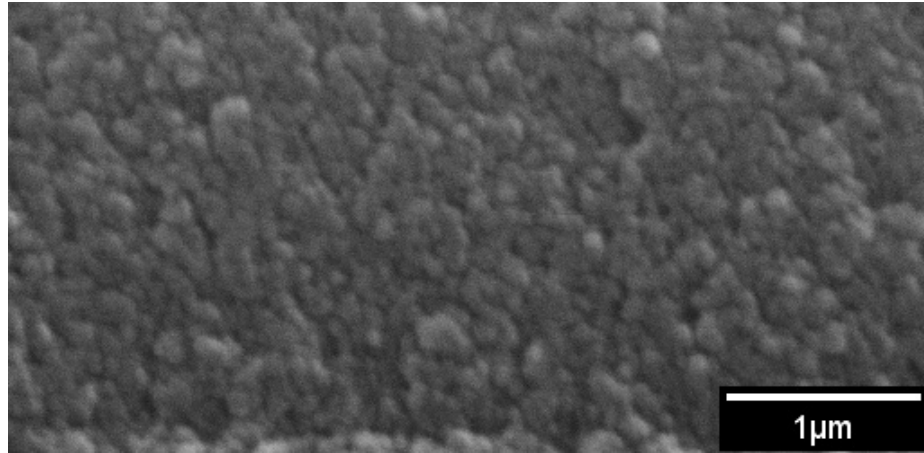
3.3.2 *n*-type Meso Porous Silicon

Anodizations of heavily doped *n*-type (111) silicon with different current densities have been performed as well. Unlike *p*-type meso porous silicon, which shows similar microstructures over a wide current density range, *n*-type meso porous silicon exhibits a significant change in morphologies as the current density changes. As shown in Figure 3.14, when the current density is low (3mA/cm²), the resulting porous silicon has really fine and highly interconnected pores. The random growth of those small pores doesn't show any direction preference. As the current density increases to 30mA/cm², the resulting porous silicon has bigger pores with a thicker silicon skeleton. This change in the morphology may contribute to the reported reduction in porosity and surface area of the resulting material as the current density increases from a low value to a medium value [24]. Further increase in the current density results in bigger pores with thinner silicon skeleton, as shown in Figure 3.14(c). It should be noted that the meso pores etched at a high current density grow preferentially along the <100> and <113> directions. A double layer structure has also been observed in *n*-type meso porous silicon with a surface layer consisting of smaller pores than the remainder of the etched layer. As shown in Figure 3.15(a), pores in the surface layer are tightly packed and grow along the direction normal to the sample surface, regardless of the crystal orientation of the substrate. The surface layer has been found to be highly stressed and susceptible to cracking and peeling. A top view of an *n*-type meso porous silicon sample with cracked surface is shown in Figure 3.15(b). For certain applications, such as using meso porous silicon as the sacrificial material in surface micro machining, where a smooth surface is essential, *p*-type meso porous silicon should be used instead to avoid the surface layer problem.

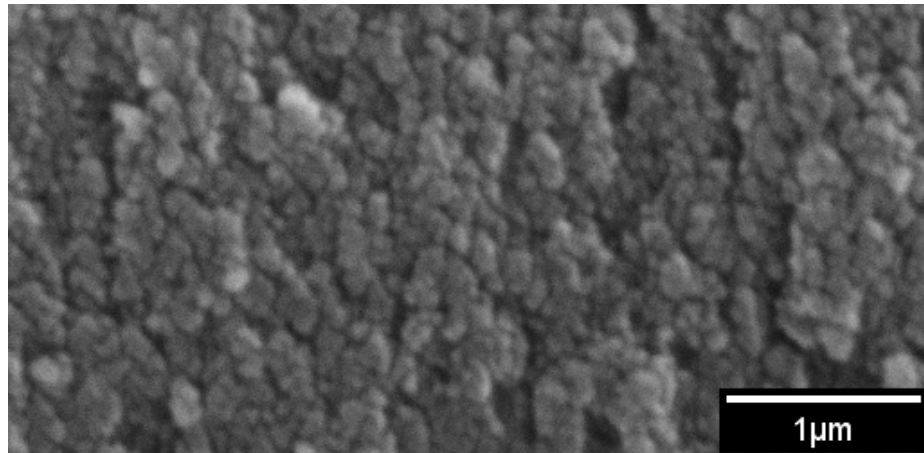
3.3.3 Formation of Thick Meso Porous Layer

Very thick PS layers are required for both the calibration source and the inlet filter. However there are several challenges associated with forming thick meso porous silicon layers. Homogeneity, for example, is very difficult to achieve when the PS layer becomes thick. As revealed in Figure 3.10, in spite of the fact that a constant current density was used, several porous layers of different porosities were formed in depth. This phenomenon is due to the depletion of reactive ions at the etching front. As the pores grow deeper, it will take longer time for ions to diffuse through the already formed porous layer. The variation in HF concentration at the interface is then faithfully reflected in the resulting porosity. If the HF concentration goes below the critical value, electropolishing instead of pore formation will occur. To improve the uniformity in depth, a lower current density can be used, so that the reaction is always limited by the transport of electronic holes. However, this method not only slows the anodization process but also sets limit on the achievable porosity. In this case, only porous layers with low porosity can be obtained. To get around this restriction, a pulsed current mode has been used. During the anodic current pause, the active species can be replenished, while the pulse amplitude can be adjusted to achieve the desired porosity. The pulsed current mode can maintain an almost constant concentration of HF in the pore tips and therefore produce a more homogeneous layer in depth. Figure 3.16 shows one of the thick PS layers that has been produced by the pulsed current mode. No apparent inhomogeneity in porosity was observed.

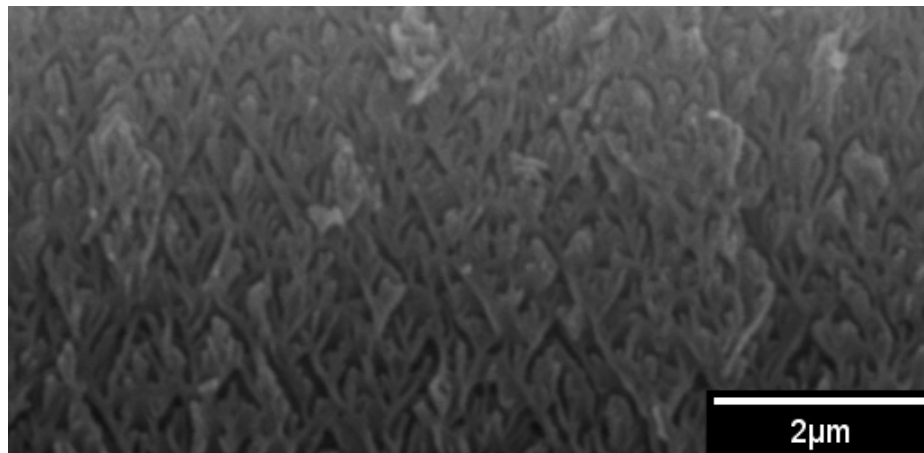
Another problem related with thick PS layer is drying. Cracking of thick PS layers has been systematically observed when water is allowed to evaporate out of the pores. Figure 3.17 shows one of the samples that cracked during drying. The origin of the cracking is due to the large capillary stresses associated with the evaporation of



(a)

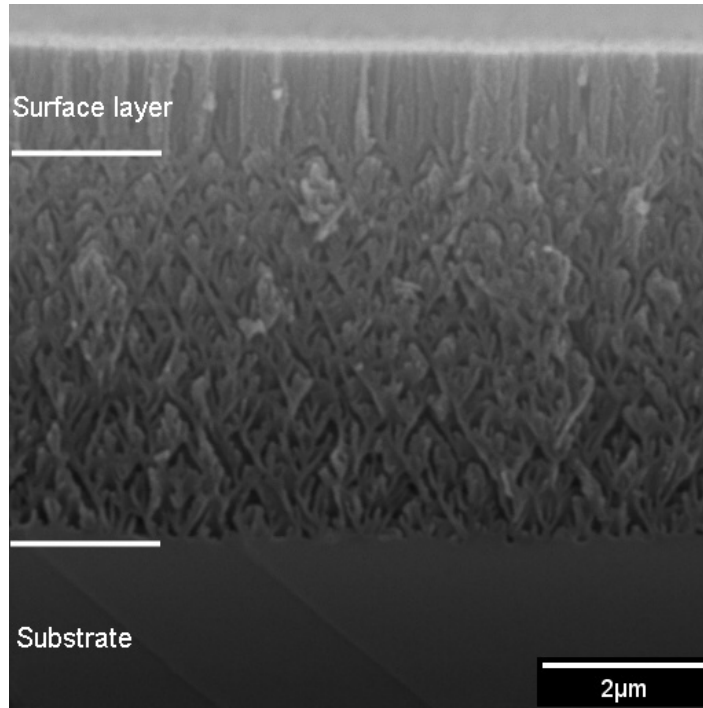


(b)

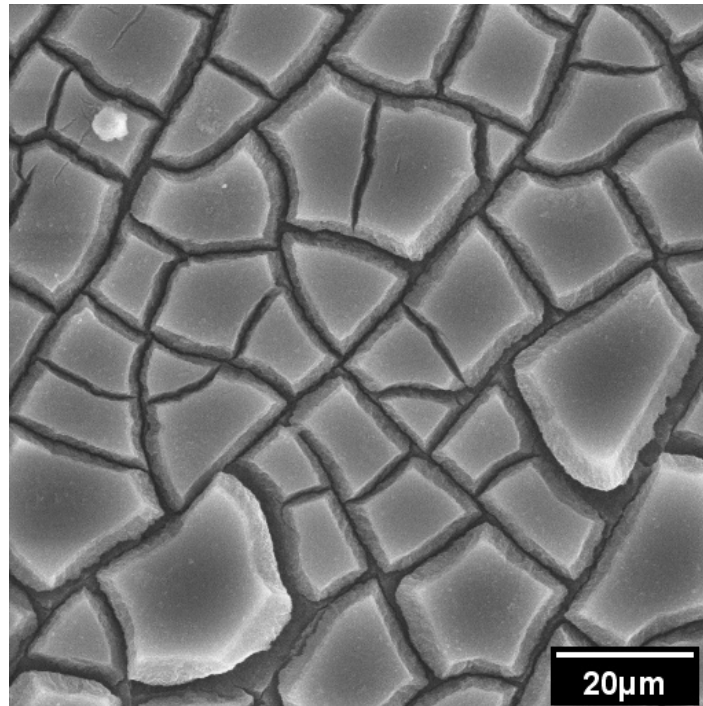


(c)

Figure 3.14: High magnification SEM photographs showing the (110) planes of mesoporous silicon layers formed in heavily doped ($0.024\text{-}0.026\Omega\text{cm}$) (111) *n*-type silicon with 12% ethanoic HF (a) at $3\text{mA}/\text{cm}^2$ (b) at $30\text{mA}/\text{cm}^2$, and (c) at $100\text{mA}/\text{cm}^2$



(a)



(b)

Figure 3.15: SEM photographs of meso porous silicon layers formed in heavily doped (0.024-0.026Ωcm) (111) *n*-type silicon; (a) the cross sectional view showing the the surface layer with small and tightly packed pores and (b) the top view showing the cracking peeling of the surface layer

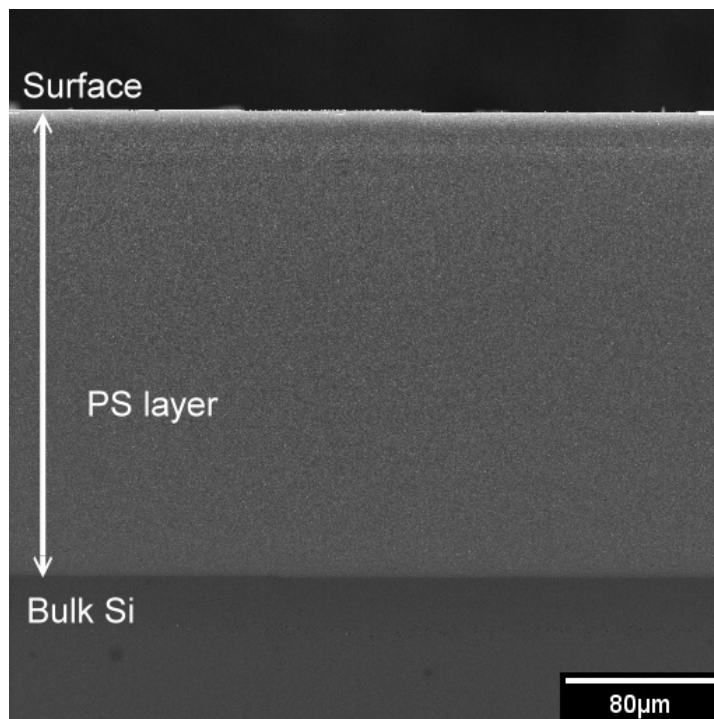


Figure 3.16: SEM photograph showing the uniform structure of the thick porous silicon layer generated by the pulsed current mode.

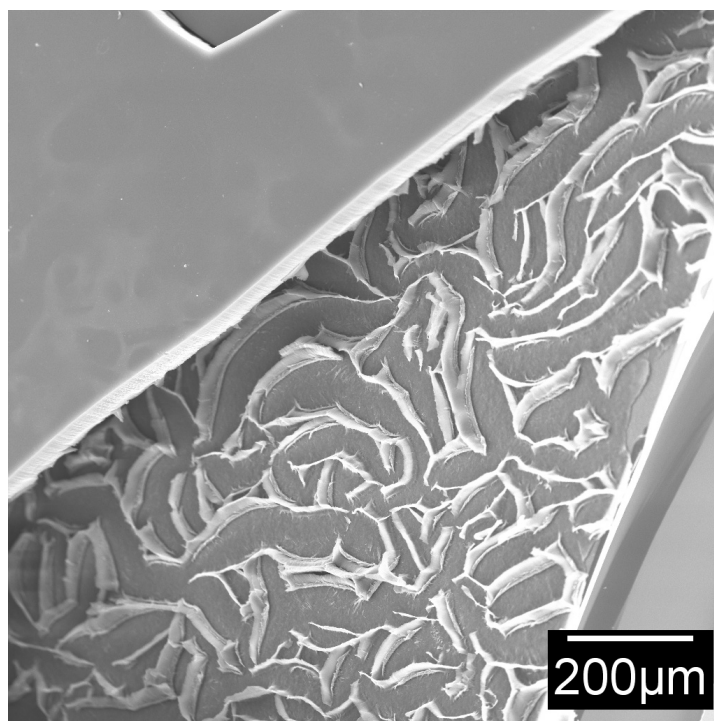


Figure 3.17: Top view of a thick meso porous silicon sample after drying with water. The porous layer was cracked during the drying

liquid in small pores [24]. This is similar to the situation when stiction occurs during a releasing of MEMS structure. To avoid such cracking, special drying methods are required. The most effective way is supercritical drying, where the transition between liquid phase and gas phase occurs above the critical point, introducing negligible surface tension. Porous layer with porosity as high as 95% has been successfully dried with this method [75]. Freeze drying has also been used for porous silicon. After PS formation, the fluid inside the pores is frozen and then sublimates under vacuum. Reported experimental results on freeze drying are not totally consistent, varying from a slight improvement [76] to a full success [77]. A relatively easy way to reduce the magnitude and effects of capillary stress is to replace water with a drying liquid of lower surface tension. Pentane, for example, has much lower surface tension (14mJ/m^2) compared to water (72mJ/m^2). Since water and pentane are non-miscible liquids, intermediate rinsing with ethanol or methanol are needed. Pentane drying is sufficient for the materials that we are interested in. The sample shown in Figure 3.16 was dried with pentane.

3.4 Macro Porous Silicon with Straight Pores

Macro porous silicon with straight pores has also been chosen as one of the candidate materials for the calibration vapor source. Since the deep macro pores have almost constant diameter through the whole depth, this type of porous silicon is expected to provide a very stable vapor generation rate over a long period of time. Methods for fabricating straight macro pores have been developed at MTU.

3.4.1 *n*-type Macro Porous Silicon

The formation of *n*-type macro porous silicon was tempted first. *n*-type (100) silicon substrates with doping levels of 0.5-1, 1-5 ,and 10-25 Ωcm were used in the inves-

tigation. The anodization was performed in an aqueous electrolyte with 4%wt HF. A drop of NC1001 (Wako) was added into the electrolyte as the wetting agent. In order to generate electric holes in the lightly doped n -type substrates, the backside of the silicon substrates was illuminated by an array of OPTEK GaAlAs infrared LED (OP295A). The wavelength spectrum of those LEDs is centered at 880nm, which matches silicon's adsorption edge. The schematic of the experimental setup is shown in Figure 3.18 [78].

Ideally, the potential across the two electrodes should be kept very low ($<5V$) to avoid electrical breakdown while the etching current density is controlled by changing the intensity of the illumination. The $J-V$ curves of lightly doped n -type silicon with illumination are shown in Figure 3.19 [44]. However, in our experiments sufficient current flows can not be consistently achieved by illumination at low bias. For most samples, a very high bias ($>60V$) was required to achieve the target etching current ($>5mA/cm^2$). The etching current density generated by the high voltage, however, would not respond to the modulation of the illumination intensity. Consequently,

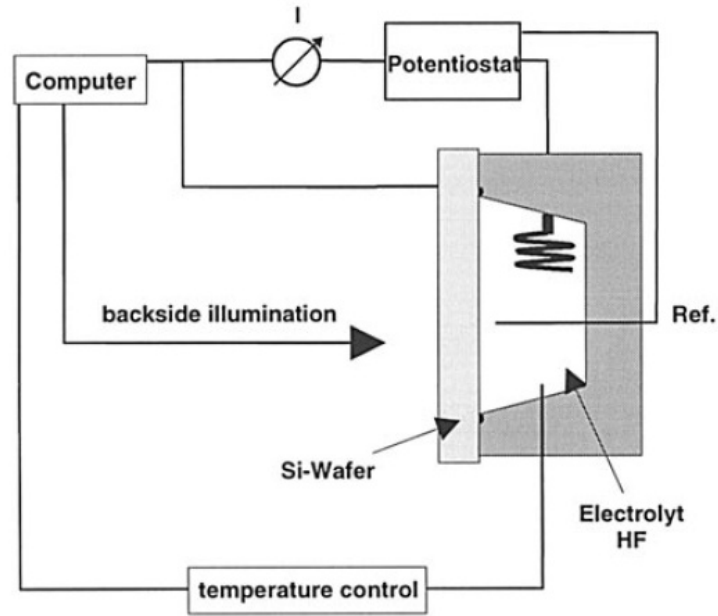


Figure 3.18: Experimental setup for the n -type macro porous silicon formation [78]

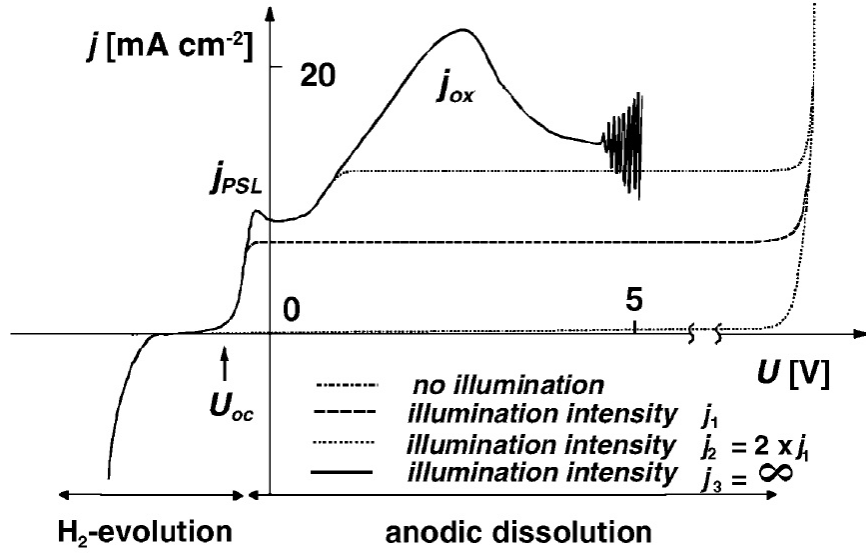


Figure 3.19: J – V characteristics of lightly doped n -type silicon in aqueous solution [44]

instead of producing nice column like macro pores, the anodization process resulted in strongly branched needle-shaped channels, as shown in Figure 3.20. As explained at the begin of this chapter, this type of porous silicon is the result of the anodization processes where hole generation is dominated by electrical breakdown at pore tips. The resulting sharp pore tips further promoted the breakdown process. Macro pores formed by photon current were observed in a few samples, as shown in Figure 3.21.

The resulting macro pores show an increase in pore diameters in depth. This is due to the increase in the etching current density reaching the pore tips as the pores grow deeper. The number of holes generated per second is directly proportional to the light intensity. Since the holes are generated at the backside of the sample, they have to diffuse toward to the pore tips as minority carriers in the n -type substrate to contribute to the electrochemical reaction. Only a part of the photon generated holes reach the front side and participate the pore formation process. Taking into account the diffusion and recombination processes in the silicon bulk, the ratio of the illumination-induced current I_{Ph} and the current reaching the pore tips I_{etch} is

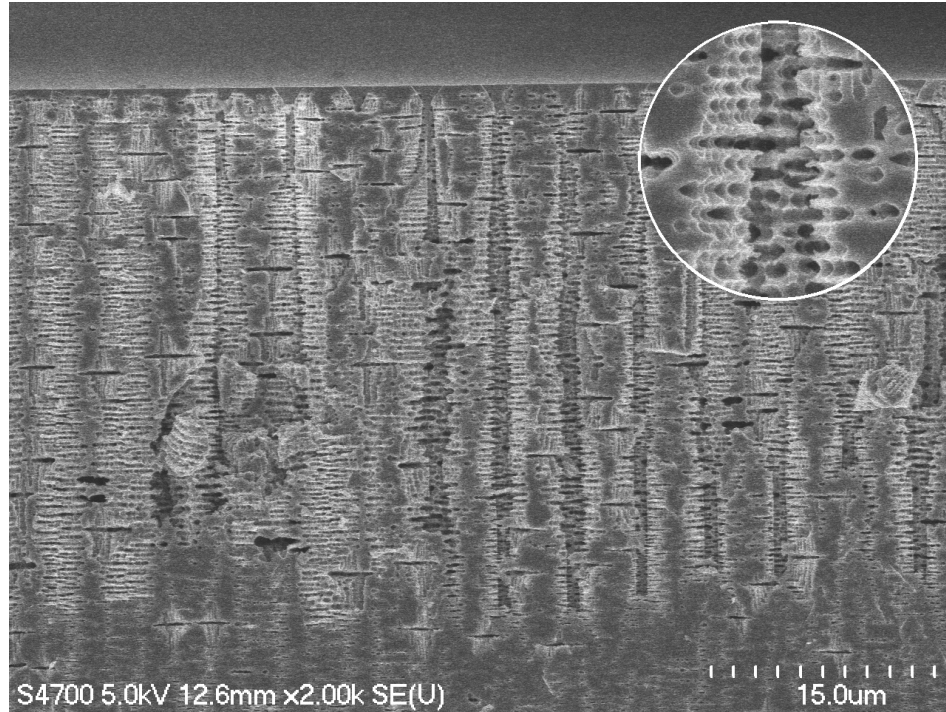


Figure 3.20: Cross section of an *n*-type (100) silicon sample (1-5 Ω cm), showing strongly branched trenches with sharp tips. It was generated by breakdown current at a very high bias (>60V).

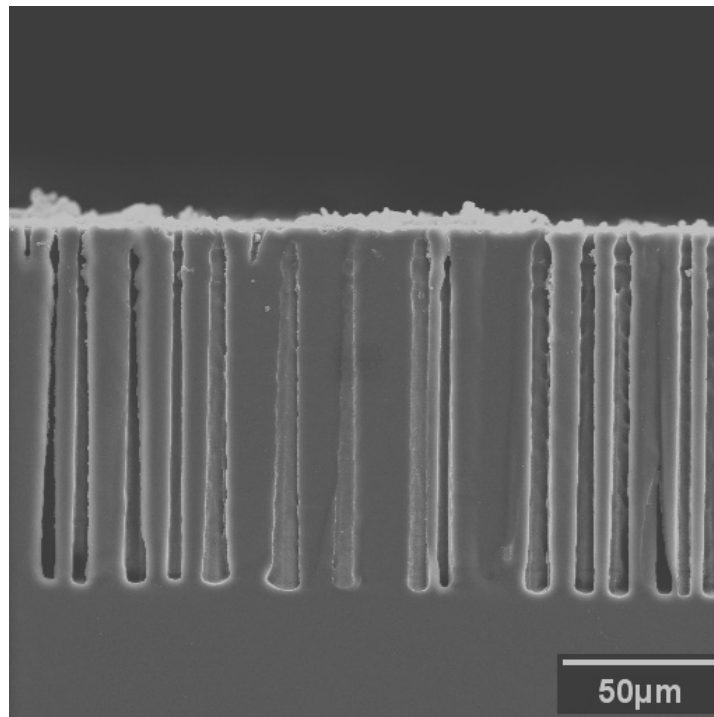


Figure 3.21: Cross section of an *n*-type (100) silicon sample (10-25 Ω cm), showing a random pattern of macro pores generated by photon current with a bias of 4V.

approximately given by the following equation:

$$\frac{I_{Ph}}{I_{etch}} \approx \cosh\left(\frac{d_w - l}{L}\right) \approx \exp\left(\frac{d_w}{L}\right) \exp\left(\frac{-l}{L}\right) \quad (3.5)$$

where L is the diffusion length, d_w is the thickness of the wafer, and l is the length of the pores. As the pores grow deeper (l increases), the distance that the holes have to travel ($d_w - l$) reduces, which results in an increase in the etching current I_{etch} , given a constant illumination intensity, i.e. constant I_{Ph} . As a result, the pore diameter increases in depth. Straight pores with constant diameter in depth can be obtained by exponentially reducing the intensity of the illumination to compensate for the change in the diffusion length of the photon generated holes [78].

Based on the collected information, it is believed that the insufficient photon current in most samples was due to a short life time of minority carriers, and therefore a short diffusion length of minority carriers in the substrate. In silicon, the minority carrier's life time is dominated by defects, impurities, and any crystal imperfections. It is thus a property that can vary over many orders of magnitude between different wafers or different locations on the same wafer. Diffusing through the whole thickness of substrate ($\sim 500\mu\text{m}$) requires a minority carrier life time around $200\mu\text{s}$ [79]. Normal n -type substrates with a resistivity around $10\Omega\text{cm}$ have a minority carrier life time on the order of $10\mu\text{s}$. However, minute amounts of impurities, such as heavy metals, are sufficient to degrade the life time far below this level. For example, a gold concentration of 10^{15}cm^{-3} can reduce the minority carrier life time to $0.1\mu\text{s}$. Since most wafer vendors don't provide information about diffusion length or life time of the minority carrier for their wafers, it is very difficult to obtain the appropriate silicon substrate for n -type macro porous silicon formation.

3.4.2 *p*-type Macro Porous Silicon

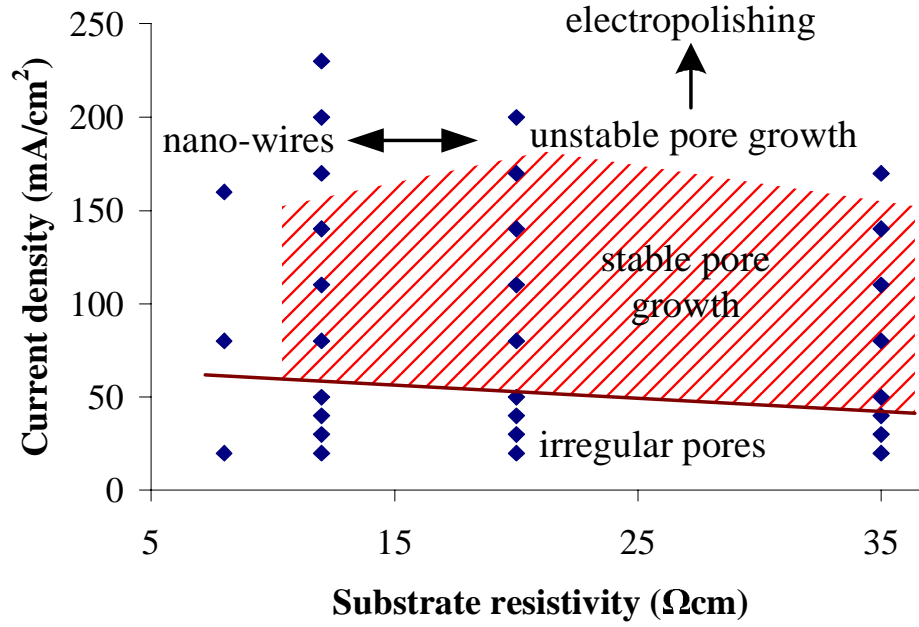
Due to the difficulty in obtaining high quality silicon wafers with an excellent minority carrier diffusion length for the *n*-type macro porous silicon formation, *p*-type silicon was studied to provide a similar macro pore structure. The *p*-Si-HF system has several advantages compared to the *n*-Si-HF system. First, it does not have strict requirements on the carrier diffusion length of the substrate. Normal prime grade wafers are sufficient for the *p*-type macro pore formation. Secondly, it does not need the backside illumination and the corresponding control system to maintain the constant photon current. Therefore, the experimental setup for the *p*-type material is relatively simple compared to those for the *n*-type macro pores. Thirdly, the etch rate of the *p*-Si-HF system is usually higher than the *n*-Si-HF system. However, the *p*-type macro porous silicon has disadvantages as well. The *p*-Si-HF system is known for its very small processing window. This is because the *p*-Si-HF system does not have the controls over the hole supply that are available in the *n*-Si-HF system through the backside illumination, diffusion and pore tip collection. Neither does the *p*-type system have the strong passivation mechanism provided by thick SCR layers as in the *n*-type system. The actual formation mechanism for *p*-type macro pore is still under discussion. But it has been agreed that every parameter has to be just right to produce good *p*-type macro pores. Since the *p*-Si-HF system is very sensitive to variations in the processing parameters, a slight decrease in HF concentration will drive the system from pore formation into electropolishing, which makes fabricating thick macro PS layers in *p*-type silicon a very challenging task.

In order to obtain stable growth of deep macro pores in *p*-type silicon, a full factorial experiment has been performed to study the impact of anodization parameters, including substrate resistivity, current density, and electrolyte composition, on the morphology and the etch rate of the resulting porous silicon. The starting materials in the investigation were *p*-type (100) prime-grade silicon substrates with doping

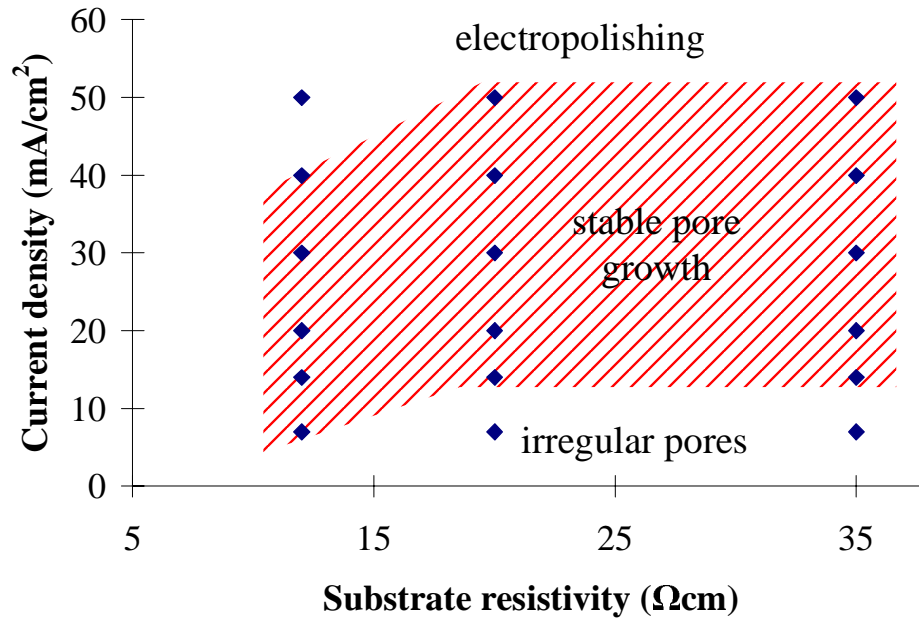
levels of 8-9, 11-12, 17-23, and 35-40 Ω cm. The experiments were carried out in the double-tank cell with Pt electrodes. Aqueous electrolytes were studied first. The electrolyte was pumped through both chambers and the anodization was performed in the dark. Two types etching solutions with HF (49%), ethanol, H₂O at volume ratio 1:1:1 and 1:2:3 were used. 10⁻³M cetyltrimethylammonium chloride (CTAC) was added to both solutions as a surfactant [43]. The same solution was used to form an electrolytic backside contact. Etching current densities from 7 to 230 mA/cm² have been studied. The etched samples were cleaved and observed using scanning electron microscopy. The cleavage plane in each cross section is the (110) silicon plane.

The experimental matrices are shown in Figure 3.22. Typical SEM images of the resulting materials are shown in Figure 3.23. Stable macropore formation is only observed in the shaded area. At the low substrate resistivity end (<10 Ω cm), only micro PS or nano-wires can be achieved, as shown in Figure 3.23(a). As the substrate resistivity increases, there forms a window for the etch current density where good macro PS can be achieved, as shown in Figure 3.23(b). If the current density is lower than the minimum value defined by the window, resulting pores are irregular, as shown in Figure 3.23(c). The wall structure is rough and side branches can be observed in some samples. If the current density is higher than the maximum value defined by the window, the wall of resulting pores becomes very thin and pore growth becomes unstable, as shown in Figure 3.23(d). Increasing the current density further will cause electropolishing. The transition between irregular macropore growth, straight macropore growth, and unstable macropore growth is gradual and the boundary for stable macropore formation was decided qualitatively. For stable macropore formation, it is desirable to use a current density in the middle of the operation window.

The etch rate of the macro pores as a function of the current density is presented in Figure 3.24. For both electrolytes, there is a monotonic increase of pore depth with current density for the same amount of anodization time. The slight nonlinearity



(a)



(b)

Figure 3.22: Experimental matrix showing stable pore growth region in (a) 1:1:1 electrolyte and (b) 1:2:3 electrolyte. Plain *p*-type (100) Si samples were anodized for 60min.

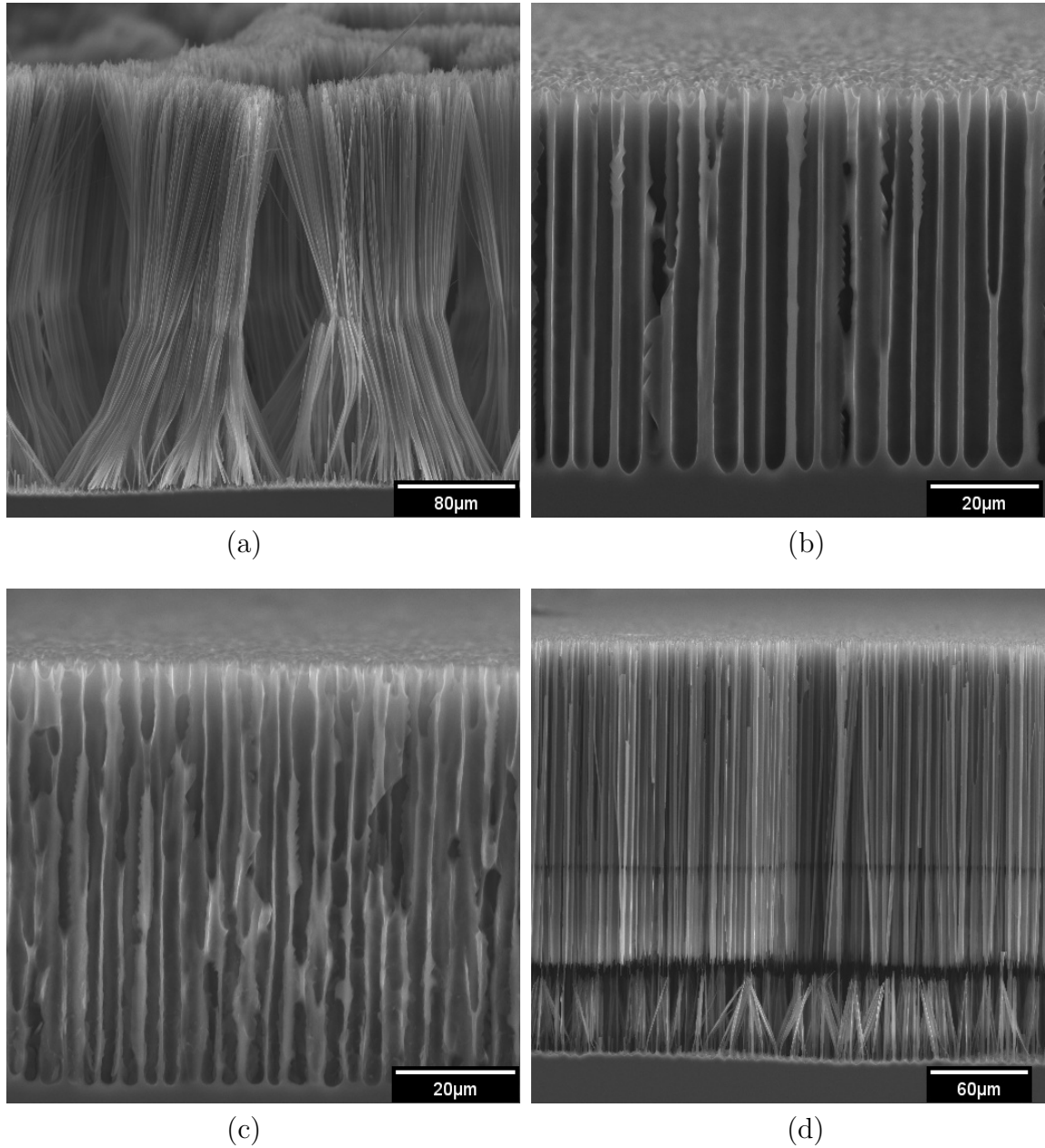
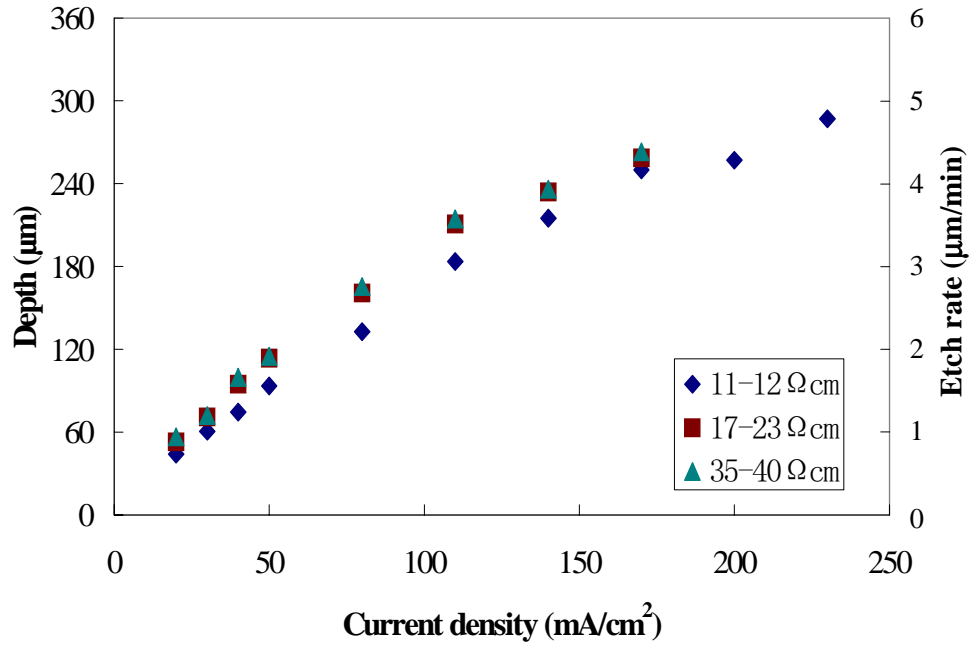


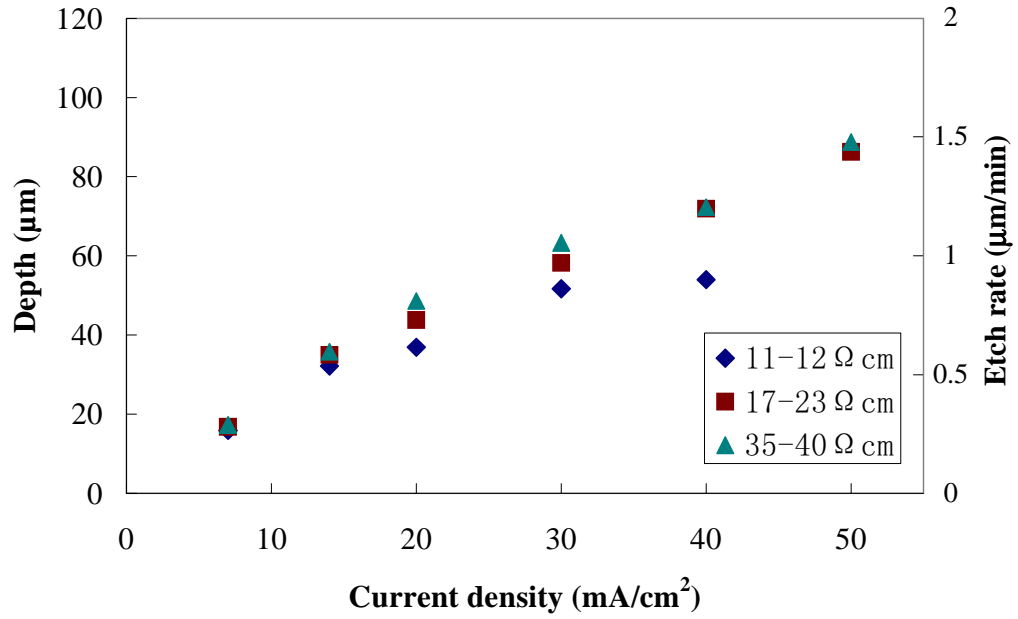
Figure 3.23: SEM photographs of the anodized *p*-type (100) silicon substrates showing (a) nano-wires obtained in the substrates with low resistivity ($9\Omega\text{cm}$ substrate etched in the 1:1:1 electrolyte at $230\text{mA}/\text{cm}^2$ for 60mins), (b) good macro pores obtained with optimal etching conditions ($17\text{-}23\Omega\text{cm}$ substrate etched in the 1:2:3 electrolyte at $30\text{mA}/\text{cm}^2$ for 60min), (c) irregular macro pores obtained with a low current density ($17\text{-}23\Omega\text{cm}$ substrate etched in the 1:1:1 electrolyte at $30\text{mA}/\text{cm}^2$ for 60min), and (d) macro pores etched with a high current density, showing very thin walls. The bottom region is partially electropolished. ($17\text{-}23\Omega\text{cm}$ substrate etched in the 1:1:1 electrolyte at $200\text{mA}/\text{cm}^2$ for 60min)

in the relationship is due to the thinning of the wall as current density increases. Figure 3.24 also shows the impact of the substrate resistivity on the etch rate. Inside the operation window, a significant increase of the etch rate was observed when the substrate resistivity increased from 11-12 Ω cm to 17-23 Ω cm. Further increases in the resistivity only cause a minor increase in the etch rate. The change in the etch rate is due to the change in the “porosity” of macro PS as the resistivity increases. Substrates with a high resistivity generate macro pores with thicker walls, which effectively reduces the total pore area. Therefore, for the same over all current density, the effective current density (current density per unit pore area) increases with the substrate resistivity, which results in a higher etch rate in the substrate with a higher resistivity.

Another important anodization parameter is the electrolyte composition, especially the HF concentration. By comparing Figure 3.22 (a) and (b), it can be observed that a higher HF concentration allows using a higher current density for macropore formation, which also results in a higher pore etch rate. The highest etch rate achieved in our experimental matrix is more than 4 μ m/min, which is very appealing from a manufacturer’s point of view. However, there are problems related with using a high HF concentration. The macro pores etched in the electrolyte with a high HF concentration tend to have relatively rough walls. Some of those pores will be filled with micro PS structures, as shown in Figure 3.25. In addition, a high etch rate corresponds to a very fast reaction rate, which can cause variation of the electrolyte concentration at the pore tips due to the limited diffusion of the electrolyte and produces unstable pore growth. A lower etch rate, on the other hand, provides more stable pore growth and produces macro pore structures with better mechanical strength. A good trade-off between etch rate, morphology and mechanical strength was achieved by using the 1:2:3 solution and a current density of 27mA/cm², resulting in an etch rate around 0.95 μ m/min in a 17-23 Ω cm substrate. The random macro pores produced by this

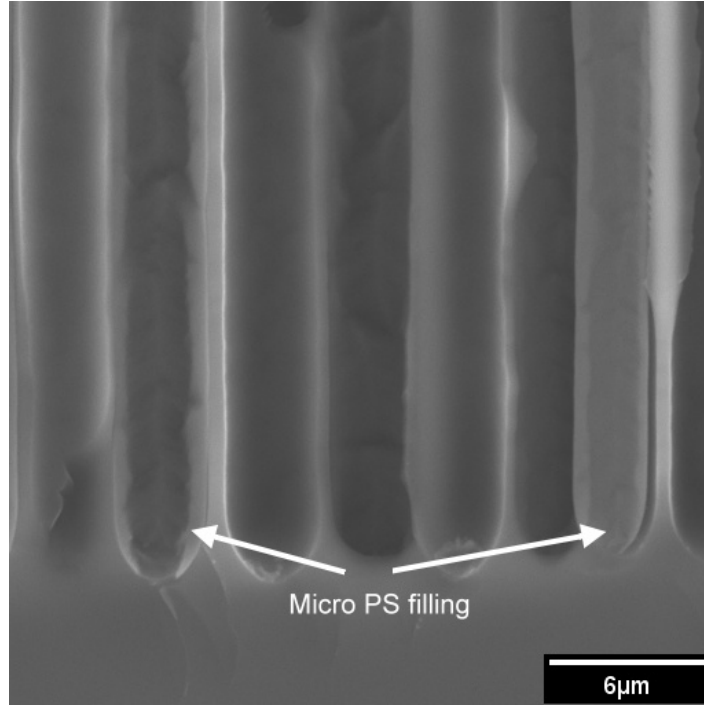


(a)

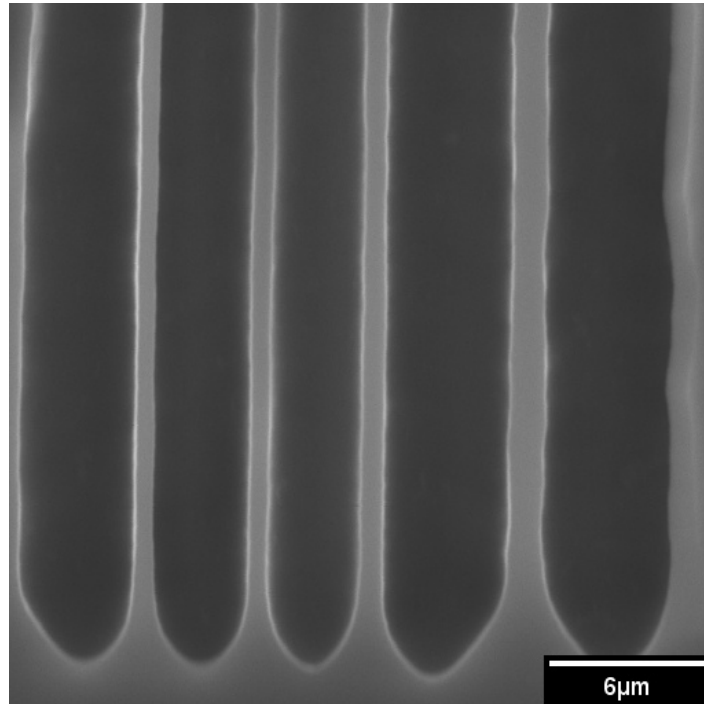


(b)

Figure 3.24: Pore etch rate as functions of current density in (a) 1:1:1 electrolyte and (b) 1:2:3 electrolyte. Plain *p*-type (100) Si samples were anodized for 60min.



(a)



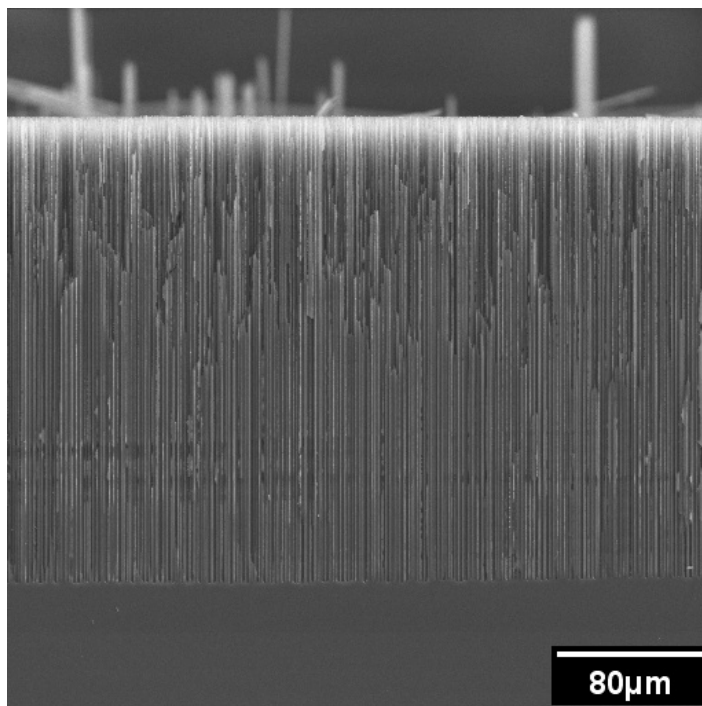
(b)

Figure 3.25: SEM photographs of macro porous silicon layers formed in 17-23Ωcm (100) *p*-type silicon substrate showing that (a) the high HF concentration (1:1:1 solution) producing macro pores with macro PS filling and rough walls, while (b) the low HF concentration (1:2:3 solution) producing clean pores with smooth walls

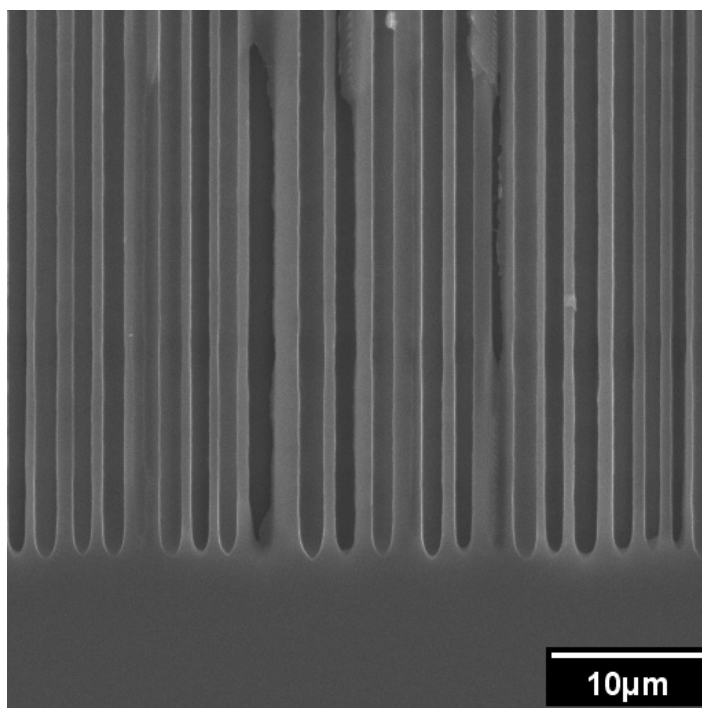
condition have an average pore diameter of $3\pm0.6\mu\text{m}$.

In order to have a better understanding of the influence that the electrolyte composition has on the anodization process, organic based electrolytes consisting of HF (49%) and dimethylsulfoxide (DMSO) at different ratios were also used in this study. Compared to the aqueous solution, the organic based electrolyte has a much lower water concentration. Since water has a very strong “oxidizing power” and promotes anodic oxidation [80], the reduction of water percentage is expected to make a difference in the anodization process.

There are several things that were noticed in our experiments with the organic electrolytes. First, similar to the aqueous electrolytes, there exists a range of current densities by which good macro PS can be achieved in the organic electrolyte. However, the requirement for the substrate resistivity is lower for the organic electrolytes. Good macro pores have been obtained in the substrate with a resistivity of $8\text{-}9\Omega\text{cm}$, as shown in Figure 3.26(a). Secondly, the resulting materials have smaller pores than those produced by aqueous electrolytes. The average pore size is about $1.1\mu\text{m}$, as shown in Figure 3.26 (b). Thirdly, the etch rates of the macro pore in the organic based electrolyte are lower than the etch rates obtained in the aqueous electrolyte. With similar HF concentrations, the organic based electrolyte can only support half as much of the anodization current density as the aqueous electrolyte does without causing electropolishing. This is probably due to the lower HF dissociation degree in the organic solution. The etch rate in the organic electrolyte, therefore, is limited by the maximum usable current density. Finally, the anodization process in the organic electrolyte has a very strong tendency to oscillate between electropolishing and macropore formation. It is partially due to the the small pore size, which limits the diffusion of active ions. Wettability of the surface and generation of bubbles may also contribute to the unstable process. Since the organic electrolyte has a slow etch rate and tends to cause unstable pore growth, it is not suitable for generating very



(a)



(b)

Figure 3.26: SEM photographs of macro porous silicon layer formed in 8-9 Ω cm (100) *p*-type silicon substrate with organic based electrolyte (DMSO:HF = 4:1) at 18mA/cm² for 6 hours. (a) The whole porous silicon layer; (b) the close-up SEM of the bottom of the PS layer, showing the details of the macropores

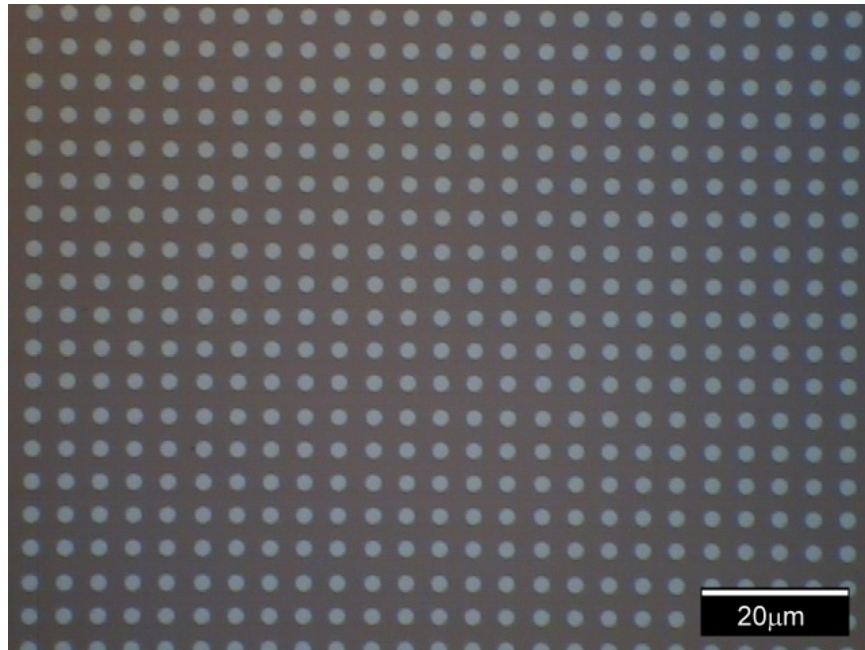
deep pores. The deepest macro pores that have been achieved with organic electrolyte in this study is $250\mu\text{m}$.

3.4.3 Size Control of *p*-type Macro Pores

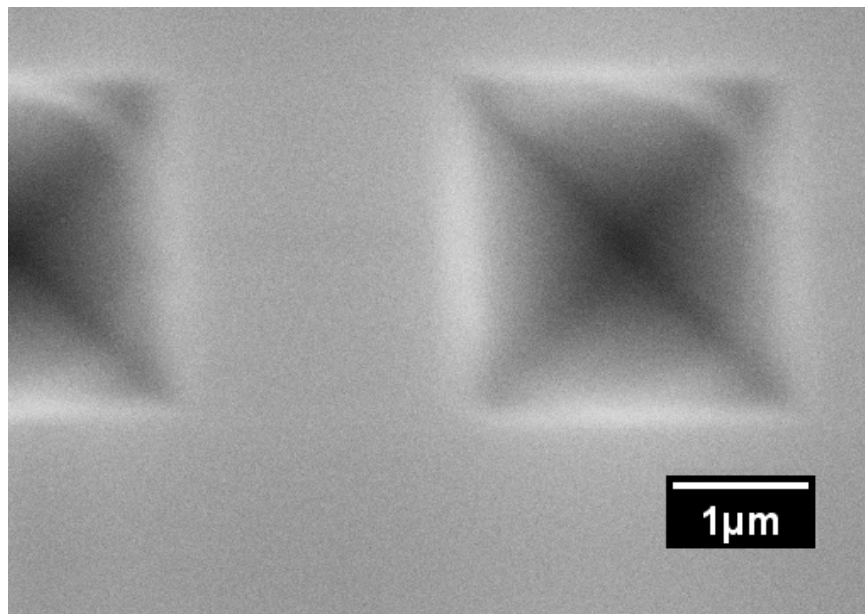
For most applications, it is desirable to have controllable pore size with tight distribution. For the *n*-type macro pores, pore size control can be obtained by modulating the photon current density. Higher current density results in larger macro pores. By changing current density during the anodization process, the size of the *n*-type macro pores can be modulated in depth. However, this method does not work for the *p*-type macro pores. In order to generate good *p*-type macro pores, the etching current density has to be in the operation window. As current density varies from the low end to the high end of the operation window, the etch rate increases. The wall thickness of the macropore becomes thinner as the current increases. However this only results in a slight increase in the pore size.

In order to obtain better control of the pore size for the *p*-type macro pores, initiating pores by pre-structuring the sample surface was studied. Standard photolithography and subsequent KOH etching were used to form arrays of inverted pyramid pits as initial pores. One of the mask patterns is shown in Figure 3.27 (a). A thin layer of oxide is used as the mask material for the KOH etching. The inverted pyramid pits are shown in Figure 3.27 (b).

Four different unit cell sizes (spacing between the nearest pits) were used to investigate the pre-structuring's impact on the macropore formation. Table 3.1 lists the unit cell sizes, the resulting pore sizes, and the corresponding etch rates. Images of the macro pores produced with pre-structured samples are shown in Figure 3.28. Instead of growing randomly, as on the plain substrate, macro pores on the pre-structured sample followed the pattern determined by those initial pits. In this ways, regular array of macro pores with very uniform pore size was obtained. The resulting pore



(a)



(b)

Figure 3.27: (a) Microscope image of the mask pattern used to pre-structure the sample surface. (b) SEM image of the inverted pyramid pits form by KOH etching in (100) sample with oxide mask.

Table 3.1: Influence of the unit cell size on the pore size and pore depth. *p*-type Si (100) 17-23Ωcm anodized for 120min under 27mA/cm² current density in the 1:2:3 electrolyte with 10⁻³M CTAC.

Unit cell size (μm)	Pore size (μm)	Pore depth (μm)
3.2	2.5	134
4.8	3.7	130
6.4	4.8	117
8.5	5.6	110

size and wall thickness were self adjusted to the unit cell size. By varying the unit cell size from 3.2μm to 8.5μm, the resulting pore size can vary from 2.5μm to 5.6μm. In this experiment, the minimum achievable pore size was limited by the lithography and subsequent etching steps. To produce array patterns with smaller unit cell size requires generating new masks with smaller feature sizes, which can be very expensive. In addition, with our current lithography capability, it will be very difficult to achieve smaller feature sizes reliably. An alternative way to generate regular array patterns without making new photo masks is Laser Interference Lithography. It makes use of laser beam interference to produce a standing wave, which can be recorded in a photoresist. Features on the order of 100nm can be obtained from UV wavelengths, and features as small as 30–40nm can be obtained from a deep UV ArF laser [81].

It's worth notice that all the samples in Figure 3.28 were produced at the same current density, which means that macro pores of different sizes can be etched at the same time on the same wafer. Although the depth of the resulting pores may vary a little bit, as shown in Table 3.1, the ability to incorporate arrays of pores with different sizes still will provide great design flexibility. Pre-structuring the sample surface not only provides a way to control the pore size, but also helps to stabilize the pore growth. With the surface pre-structuring and an optimized anodization condition (a substrate resistivity of 17-23Ωcm, a current density of 27mA/cm², and

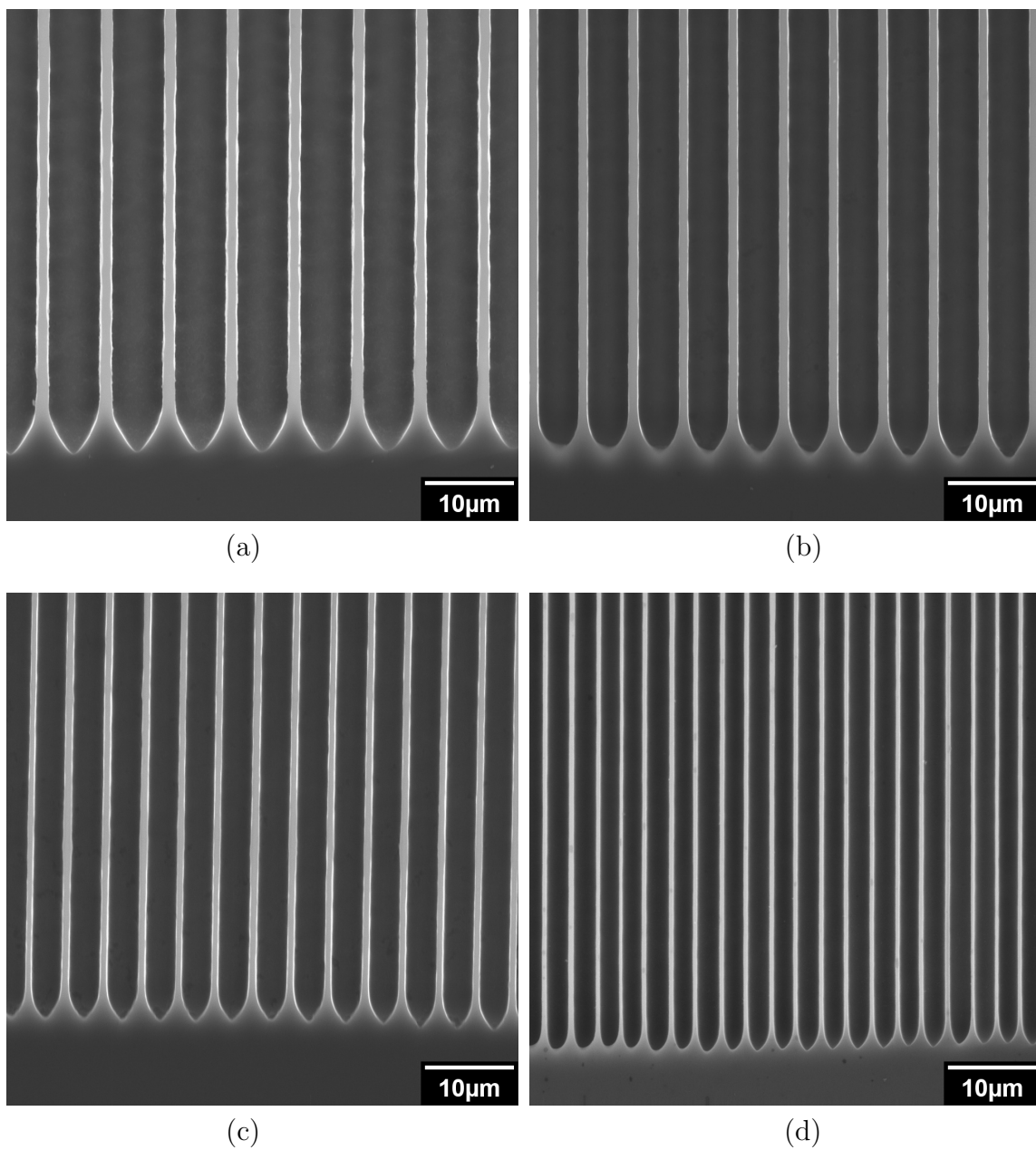


Figure 3.28: SEM photographs of the *p*-type macro pores formed from pre-structured substrates with unit cell size of (a) $8.5\mu\text{m}$, (b) $6.4\mu\text{m}$, (c) $4.8\mu\text{m}$, and (b) $3.2\mu\text{m}$. All samples were etched in the 1:2:3 aqueous electrolyte at $27\text{mA}/\text{cm}^2$.

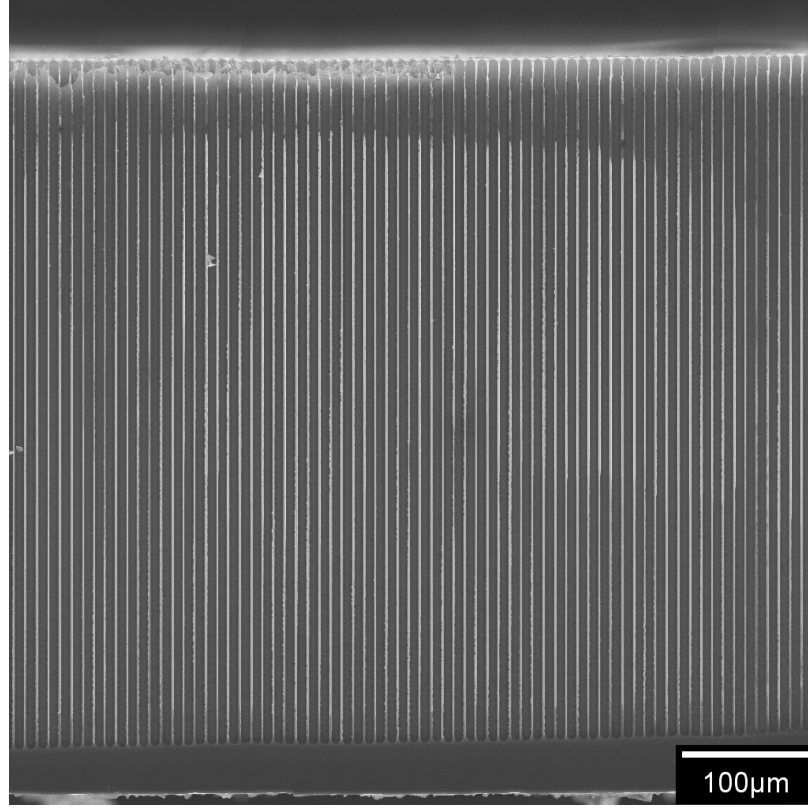


Figure 3.29: SEM photograph of a very thick *p*-type macro porous layer produced by a pre-structured sample ($17\text{-}23\Omega\text{cm}$) at $27\text{mA}/\text{cm}^2$ in the 1:2:3 electrolyte for 9 hours.

an electrolyte with HF (49%), ethanol, H_2O at volume ratio 1:2:3), we were able to produce *p*-type macro pores through the whole thickness of the silicon substrate ($>500\mu\text{m}$). To our knowledge, this is the thickest *p*-type macro porous layer that has ever been reported. SEM image of a very thick *p*-type macro porous layer is shown in Figure 3.29.

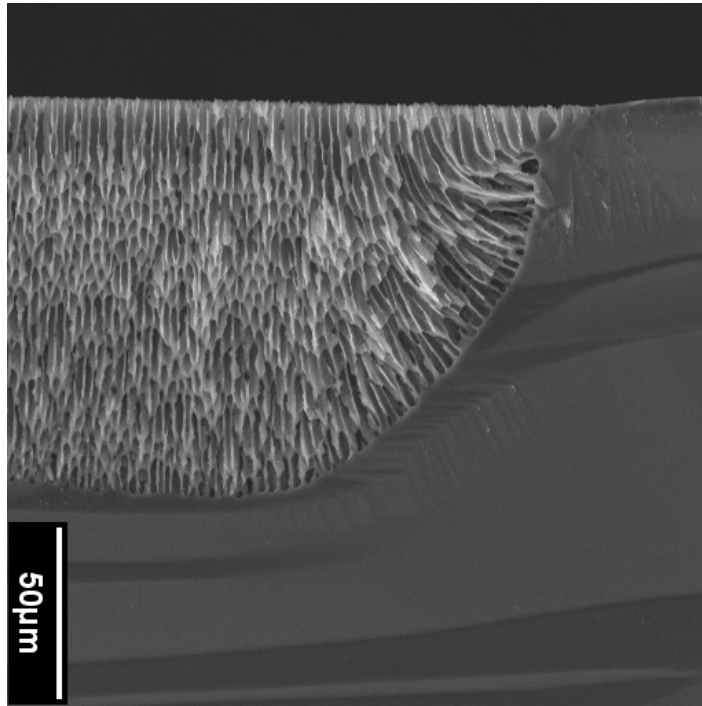
3.5 Macro Porous Silicon with Tortuous Pores

During the experimental work leading toward the optimization of *p*-type macro porous silicon with straight pores, it has been noticed that in some samples macro pores curved along the flow of current at the edge of the PS region, while in other samples macro pores at the edge branched along the $\langle 100 \rangle$ crystalline directions. The two

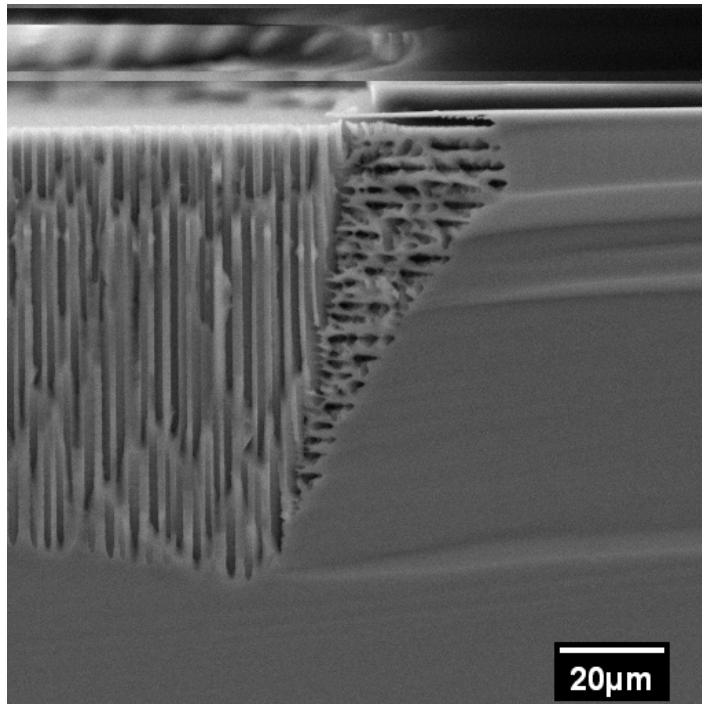
types of macro pores are shown in Figure 3.30 (a) and (b).

This interesting phenomenon has inspired us with a method to generate macro pores with different degree of tortuosity, which could be used as the inlet filter for the μ GC. Since the current flow is usually normal to the sample surface, the pore growth along the $\langle 100 \rangle$ - crystalline direction is expected to introduce the desired tortuosity. In order to maximize the achievable tortuosity by crystalline orientation dependency, the p -type (111) Si substrates with resistivity of 10-20 Ω cm was chosen as the starting material. The experiments were carried out in a conventional single-tank cell with a metallic backside contact to the Si and a Pt counter electrode. Both organic electrolytes (HF:DMSO=2:25 and 6:25) , and aqueous electrolytes (HF:ethanol:H₂O= 1:2:3) were used as the etching solutions. 10⁻³M cetyltrimethylammonium chloride (CTAC) was added into the aqueous electrolyte. Etching current densities in the range of 2 to 25 mA/cm² have been studied. The etched samples were cleaved and observed using scanning electron microscopy. The cleavage plane in cross section is the (110) silicon plane.

Crystal orientation dependent growth of macro pores was achieved with an organic electrolyte at a low HF concentration with a low current density (HF:DMSO=2:25, 2mA/cm²). Figure 3.31 (a) shows the anisotropic growth of macro pores along $\langle 100 \rangle$ - and $\langle 113 \rangle$ - directions. As the current density increases, the growth of macro pores along the current direction becomes more pronounced. Figure 3.31 (b) shows the sample etched in the 2:25 electrolyte with a current density of 5mA/cm². The resulting macro pores are no longer zig-zag shaped. Instead, they have rather smooth transitions between the $\langle 100 \rangle$ - and $\langle 113 \rangle$ - directions. As stated before, the maximum current density for macropore formation is limited by the critical current density value, beyond which electropolishing instead of macropore formation will occur. In order to increase the current density further, an electrolyte with a higher HF concentration was used. Figure 3.31 (c) shows the sample etched in the 6:25 electrolyte with



(a)



(b)

Figure 3.30: SEM photographs of the edge of PS regions showing (a) the curving of macro pores along the direction of the current flow, and (b) the branching of macro pores along the $\langle 100 \rangle$ crystalline directions

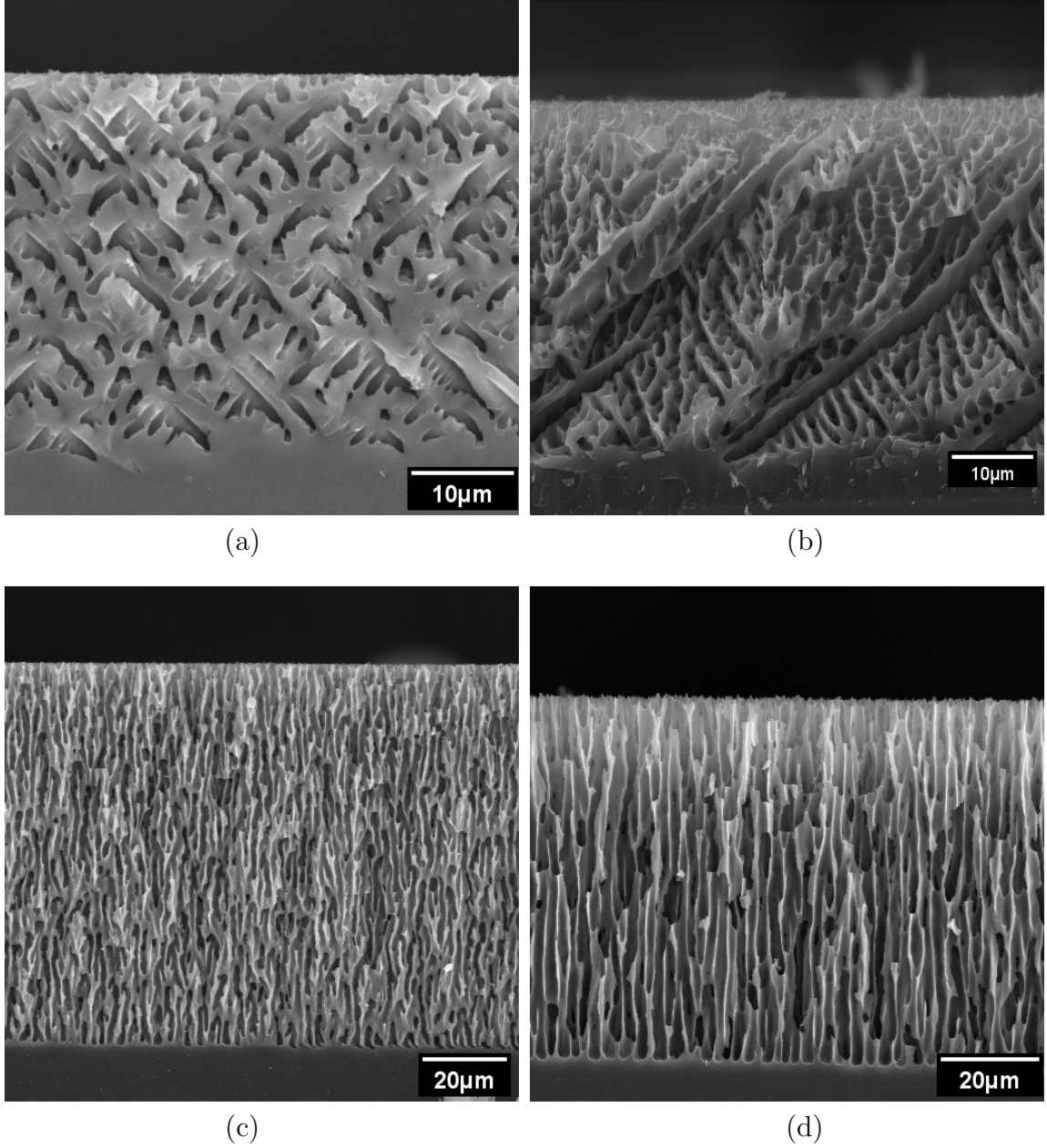


Figure 3.31: SEM images showing different macropore growth regimes, (a) crystal orientation dependent pore growth (HF:DMSO=2:25, 2mA/cm²), (b) crystal orientation dependent pore growth with enhanced current direction dependent pore growth (HF:DMSO=2:25, 5mA/cm²), (c) current direction dependent pore growth (HF:DMSO=6:25, 15mA/cm²), and (d) enhanced current direction dependent pore growth (HF:EtOH:H₂O=1:2:3, 30mA/cm²).

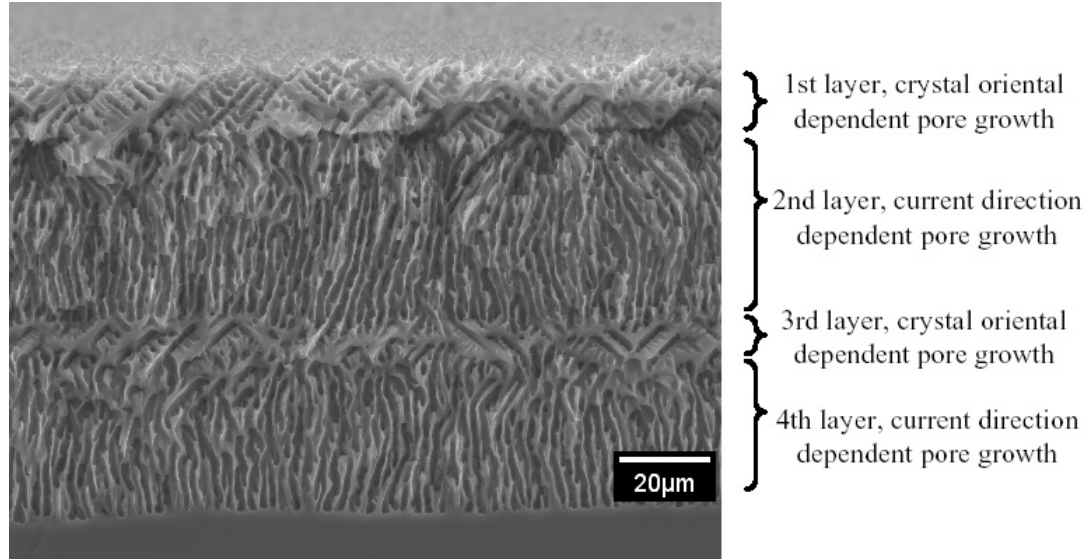


Figure 3.32: Cross section of a macro morphology superlattice structure consisting of four layers.

current density of $15\text{mA}/\text{cm}^2$. The macro pores primarily grow along the direction of the current flow, which is perpendicular to the sample surface.

The transition from the crystalline oriented pore growth to “current-oriented” pore growth can be understood as the result of the switching of the dominant reaction at the pore tip. Silicon is dissolved by two main reaction paths: the direct silicon dissolution path, where silicon reacts directly with HF and goes into solution, and a two-step dissolution path, where silicon first forms an anodic oxide layer and then the oxide is chemically dissolved by the HF. The ratio between these two reaction paths is critical for pore morphologies. If the direct dissolution path dominates, the resulting pores are faceted and grow anisotropically [69,70]. If the anodic oxidation and dissolving path dominates, the resulting pores have smooth walls and are more current oriented. The ratio and the interaction of the two dissolution paths for silicon are determined by the ability of the electrolyte to form an anodic oxide [82], the current density, and the etching temperature. By increasing the current density and/or using an electrolyte that has a higher “oxidizing power” level, the anodic oxide formation can be enhanced. It should be noted that water is a very strong

anodic oxidizing agent [80]. Since liquid HF typically includes a large percentage of water, higher HF concentration in the organic electrolyte solution not only gives higher critical current density, but also provides a higher portion of anodic oxidation in the overall reaction. That is why a smooth and more isotropic pore growth was obtained with the organic electrolyte solution at a high HF concentration and a high current density. As confirmed in Figure 3.31 (d), the macro pores etched in the aqueous electrolyte, show even stronger current direction dependent pore growth.

With the knowledge of etching conditions for macro PS with various morphologies, heterostructures can be achieved by modulating the etching conditions during the process. Figure 3.32 shows a morphology superlattice structure.

Chapter 4

Development of Integration Technologies for Porous Silicon

The development of porous silicon materials was only the first step toward a working process that produces the final device. In developing such a process for the calibration vapor source and the inlet filter, there were several key questions to be answered, including the method of forming porous silicon in predefined regions, the method of forming a porous silicon membrane with uniform thickness and the method to integrate porous silicon samples into the micro devices. The development of those supporting technologies is described in this chapter.

4.1 Localized Porous Silicon Formation

For most device applications, it is essential to be able to form porous silicon in predefined regions. Localized PS formation is usually achieved by masking a surface with a layer of etching resistant materials. For short-duration etching (less than several tens of seconds), standard photoresists can provide sufficient masking. However, when it comes to the formation of a very thick PS layer, which may require etching in HF based solution for more than 10 hours, it becomes very difficult to find an appropriate masking material. Several inorganic and organic masking layers and annealing processes have been studied as the masking material for HF etching. The masked samples were etched in 15% ethanoic HF for 3 hours. The results are summarized in

Table 4.1: Characteristics of different masking materials for porous silicon formation

Masking material	Masking Characteristics
Cr(0.1 μ m)/Au(0.3 μ m)	The metal films peeled off totally.
5 μ m SU8	The photoresist layer peeled off in most areas.
0.3 μ m sputtered Si _x N _y (without annealing)	The mask layer is severely discolored. Many large pin holes with porous silicon formed underneath can be seen at the surface.
0.3 μ m sputtered Si _x N _y (RTA 800°C for 1min)	The mask layer is slightly discolored. A few little pin holes can be seen at the surface.
SiO ₂ (0.1 μ m)/Si(0.2 μ m) (RTA 900°C for 1.5min)	The discolor of the film is negligible. A few little pin holes showed up at the surface. The mask layer was lifted up at the edge of the pattern.
SiO ₂ (0.1 μ m)/Si _x N _y (0.7 μ m) /Si(0.2 μ m) (RTA 800°C for 1min)	The discolor of the film is negligible. Very few little pin holes showed up at the surface. The mask layer stayed in place at the edge of the pattern.

Table 4.1. Both Au/Cr stack and SU8 photoresist have excellent resistance to HF. However, neither of them adhere to silicon substrate well enough to be used as the masking material. As revealed by the severe discoloring, sputtered silicon nitride film has high etch rate in HF solution. The film is also very porous, which caused a lot of pin holes. Pin holes were highlighted by the porous silicon etching. A short RTA annealing was able to improve the quality of the nitride film significantly. It not only reduced the etch rate of nitride in HF, but also decrease the pin hole density. Annealed nitride films has been found appropriate for HF etching up to a few hours. The masking stack consisting of annealed poly silicon on top of silicon dioxide showed very promising masking characteristics. No noticeable discoloring was observed. However at the pattern's edges, where undercut occurs, the masking stack buckled up and some of it was flushed away by bubbles. Damaging of the masking layer at the edge results in an extended undercut. The best masking characteristics were achieved by adding a relatively thick nitride layer in between the poly silicon and silicon dioxide layers. The existence of nitride layer modified the net stress of the masking stack, turning

it from compressive into tensile, which eliminated the buckling problem. The nitride layer also offered a good mechanical strength to withstand the flushing of evolving bubbles. No damage of the masking stack was observed at the pattern's edge any more. The tri-layer stack can be used as the mask for extremely long duration HF etching up to twenty hours.

Patterning of the tri-layer stack can be involved. The simplest method is lift-off. Futurrex negative photoresist NR1-3000PY proved to be an ideal candidate for this application. After a standard litho procedure, it yields a $3\mu\text{m}$ thick layer with undercuts, which is sufficient for the lifting off of the $1\mu\text{m}$ thick masking stack. Although the lift-off process looks very simple, special attention is needed to make it actually work. One of the major problems with the lift-off method is the processing temperature. Since the substrate holder of the 8" sputtering tool that was used to deposit the masking stack is not cooled, the temperature of the silicon substrate can go very high ($>200^\circ\text{C}$) during the deposition. If the silicon substrate prepared for the lift-off process experiences high temperature, the photoresist will get burned and can not be removed by the photoresist stripper. In order to avoid the high substrate temperature, the deposition process should be divided into several intervals and enough cooling time should be allowed between the deposition intervals. The cooling of the substrate holder is very slow in the vacuum chamber and can take several hours. A second problem of the lift-off method is related with the quality of the masking stack. The photolithography process will leave some photoresist scum in the "supposed to be clean" area. During the deposition process, the photoresist scum will be buried by the masking stack and stays there through the rest of the fabrication process. When the masking stack is being annealed, the buried photoresist scum will get burned and generates small bubbles or pin holes in the masking stack. Therefore, the lift-off method can potentially impair the integrity of the masking stack.

Since the quality of the masking stack is critical to long duration etchings, a

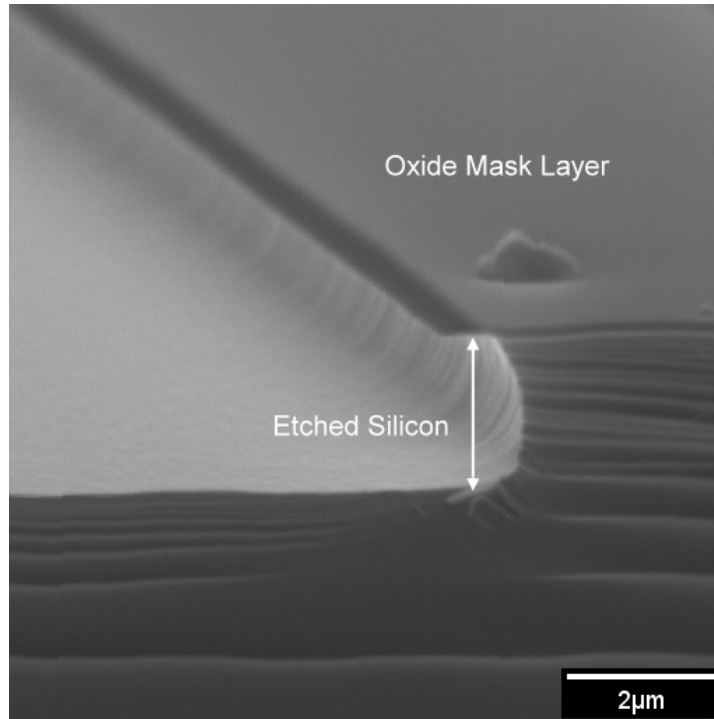


Figure 4.1: SEM photographs of a silicon substrate with oxide mask, showing the the good etch selectivity between single crystal silicon and silicon dioxide by the RIE etching (30W, SF_6 70sccm, pressure 120mTorr, 2 minutes)

combination of dry etching and wet etching has been developed to replace the lift-off process. In the new process, the poly silicon layer and silicon nitride layer were selectively etched away by Reactive Ion Etching (RIE) first, using the oxide layer as the etch stop. The oxide layer was then etched away in buffered HF solution using the already patterned poly silicon and silicon nitride layer as the etching mask. With this patterning method, the masking stack can be deposited on the clean wafer surface and the organic contamination from the photoresist underneath the masking stack is eliminated.

A very critical step of the new patterning process is the RIE etching of the silicon/nitride layers. A March Jupiter II table top parallel plate reactor was used to complete this step. The silicon/nitride layers were etched with free fluorine ions, which in our case were provided by Sulfur Hexafluoride (SF_6) plasma. In order to obtain the high selectivity, low power (30W) and relatively high pressure (SF_6 70sccm,

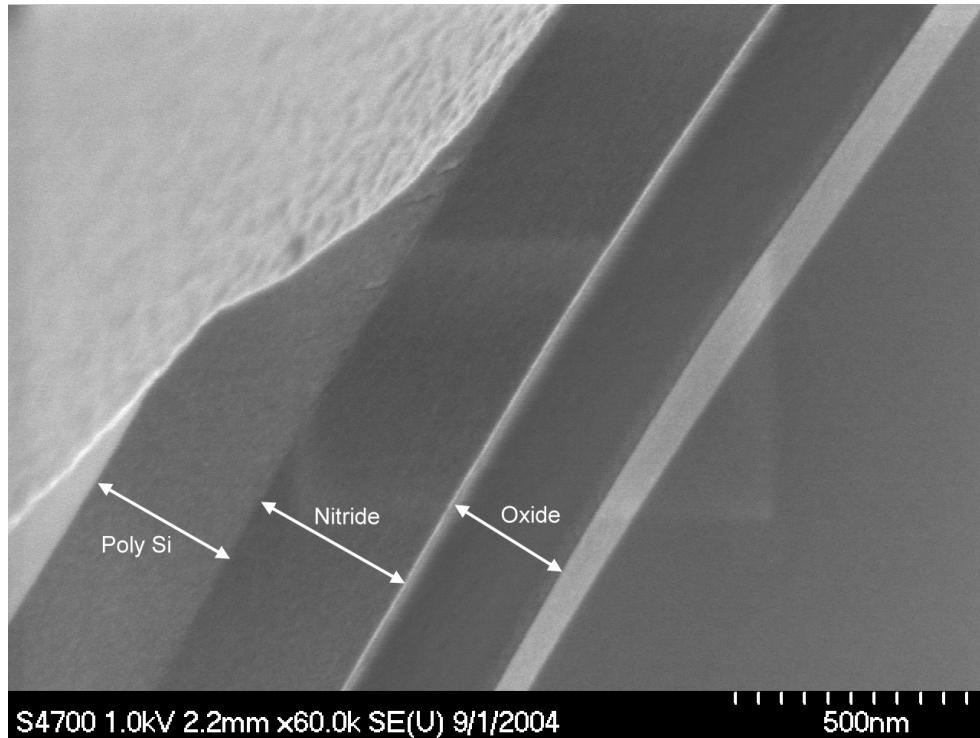


Figure 4.2: SEM photographs of silicon sample showing the RIE etching of sputtered poly silicon and silicon nitride with oxide etch stop and photoresist mask. The sample was etched at 30W and 120mTorr (SF_6 70sccm) for 3 minutes. The removal of 400nm thick poly silicon layer indicates an etch rate of 133nm/min for poly silicon etch.

pressure 120mTorr) were used to promote the reactive etching component (chemical etching) of the RIE process. The etch selectivity between single crystal silicon and oxide is demonstrated in Figure 4.1, where an oxide masked silicon substrate has been etched for 2 minutes with the above mentioned condition. While $2\mu\text{m}$ thick silicon was etched off the substrate, the thin oxide mask layer ($0.14\mu\text{m}$) remained intact. Due to the chemical nature of this etching, the resulting profile is isotropic. Undercuts can be easily observed in Figure 4.1. An extended etching revealed that a selectivity greater than 50:1 between single crystal silicon and silicon dioxide can be obtained with this etching condition. The etching of sputtered poly silicon and silicon nitride was studied as well. Si samples were sputter coated with a stack of oxide, nitride and silicon layers. Photoresist was then patterned as the etching mask. The samples were etched in RIE for 3min, 5min and 7min. The 3min etching revealed an etch rate

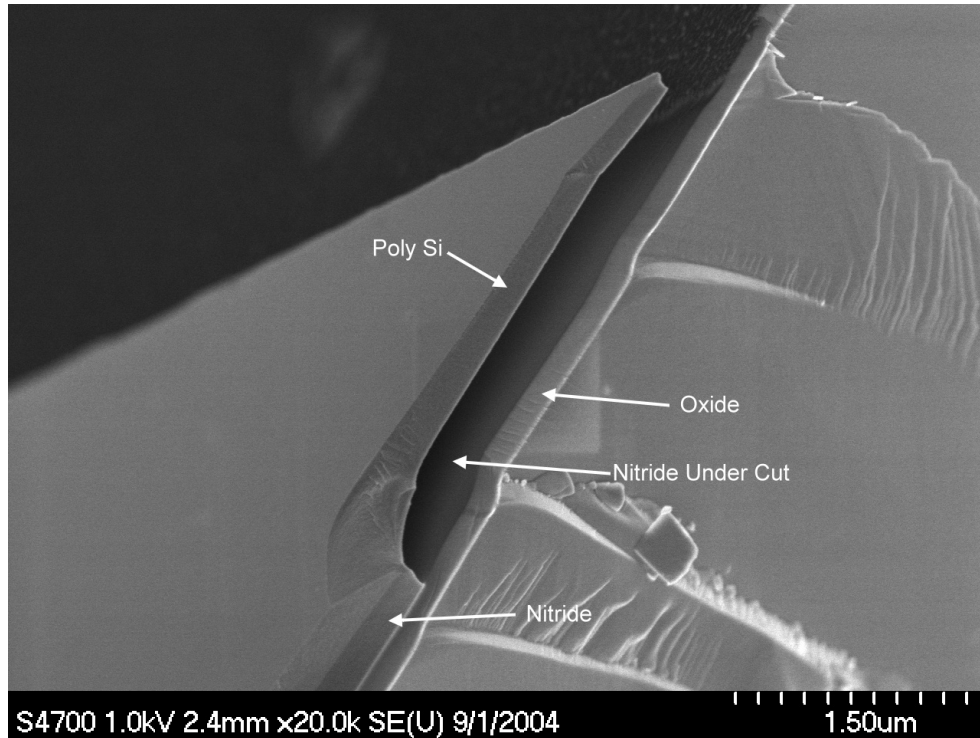


Figure 4.3: SEM photographs of silicon sample showing the RIE etching of sputtered poly silicon and silicon nitride with oxide etch stop and photoresist mask. The sample was etched at 30W and 120mTorr (SF_6 70sccm) for 7 minutes. The huge undercut indicating a very high lateral etch rate of nitride layer.

of 133nm/min for the poly silicon layer, as shown in Figure 4.2. The etch rate for the nitride layer was extremely high. After etching through the whole thickness of nitride layer in a few seconds, the RIE started to etch the nitride layer laterally at a rate of 750nm/min. A huge undercut of the nitride layer was observed after a 4min over etch, as shown in Figure 4.3. The etch rate for the oxide layer is negligible in this case, which makes oxide a very good stop layer for this etching process. Since the large undercut is not desirable for the masking purpose, the process should be carefully monitored to not over etch the masking layers. Fortunately, the end point of the etching process can be easily detected by watching the color change of the sample surface and the etching plasma. Patterning of the tri-layer masking stack has been successfully demonstrated by the RIE etching and subsequent BHF etching on 4" wafers. Figure 4.4 shows one of the 4" wafers that has porous silicon formed in

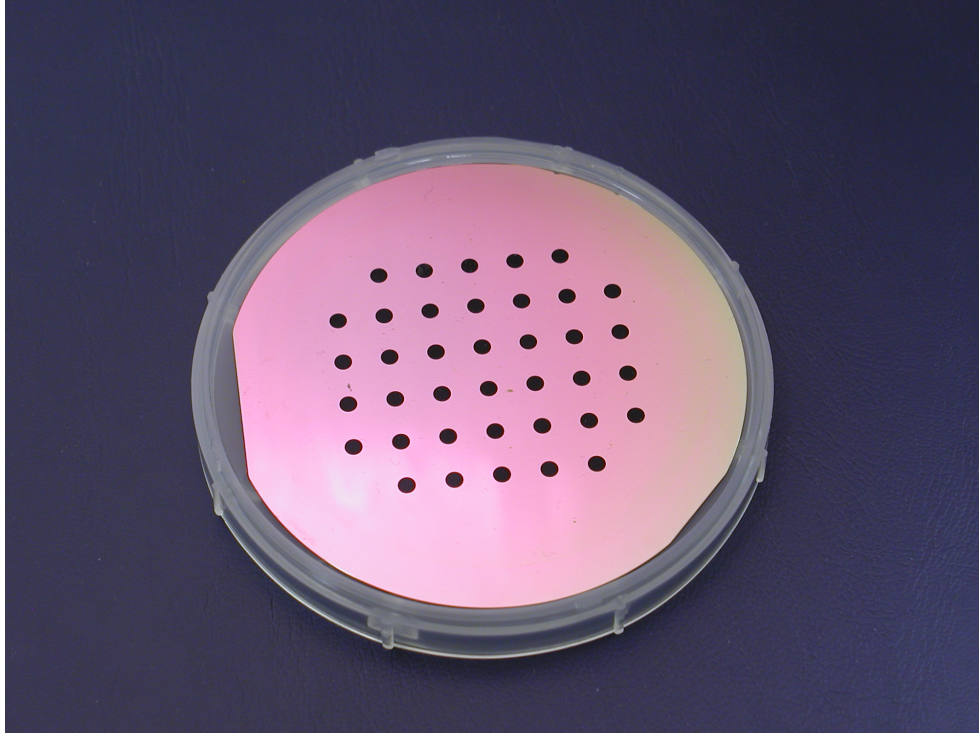


Figure 4.4: Image of a 4" wafer that has been anodized in HF based solution. The etching mask consists of oxide, nitride, and poly silicon layers. The mask stack was patterned by a combination of dry etching and wet etching.

regions defined by the patterned tri-layer etching mask.

4.2 Membrane Formation

Most micro devices not only have specific requirements on the location of the porous silicon material, but also have special requirements on the geometric form of the porous silicon material. Recently, there are an increasing number of applications call for very thick porous membranes with through pores [83, 84], among which are the calibration vapor source and the particle filter for the μ GC system. In order to obtain open ended pores, methods for forming porous silicon membranes have been developed at MTU.

At first glance, it may seem very straight forward to form open ended pores: if the anodization duration is long enough, the pores should go through the whole thickness

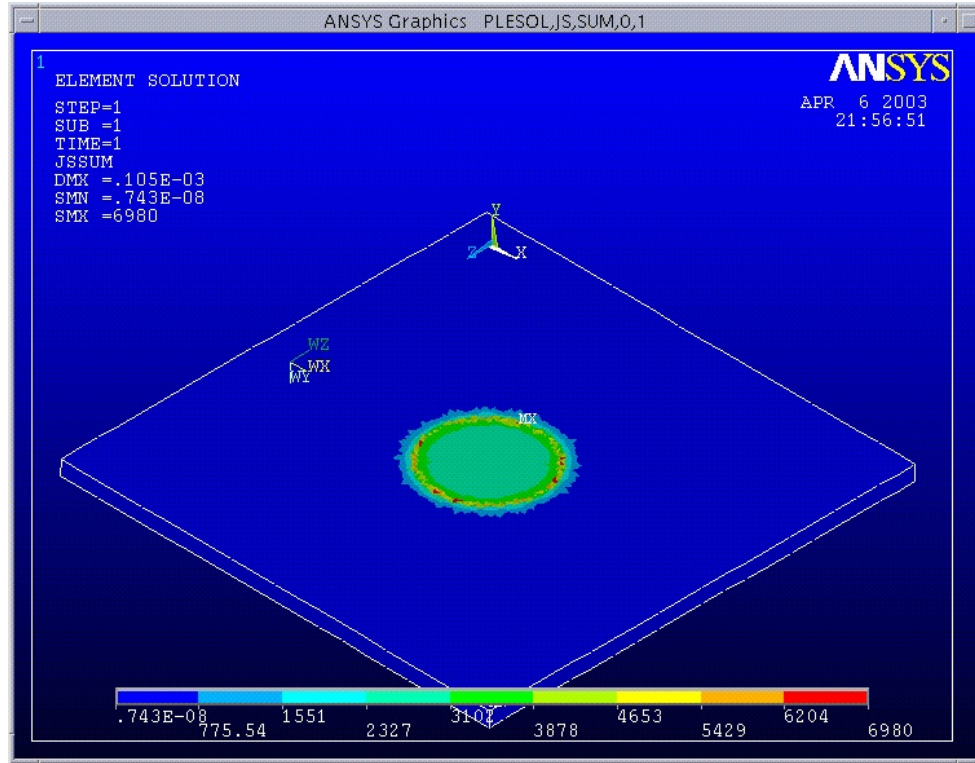


Figure 4.5: Ansys simulation of a lightly doped silicon sample ($1.5\text{cm} \times 1.5\text{cm}$ with a circular opening of 3.5mm diameter in the non-conductive mask layer) showing $>50\%$ increase in the current density at the edge of the pattern

of the sample. However, this is not the case for porous silicon formation. Due to the passivation mechanisms that prevent pore walls being etched, there will be a thin layer of crystalline silicon left at the backside of the silicon sample even after an extended anodization process. Removing this crystalline Si layer without damaging the porous silicon structure is a very tricky task.

The process to form a porous silicon membrane is further complicated by localized PS formation. The existence of etching masks causes a non-uniform current distribution across the sample surface. Due to the current crowding effect, peripheral areas of a pattern always see a higher current density. A simple Ansys simulation of a silicon sample ($1.5\text{cm} \times 1.5\text{cm}$ with a circular opening of 3.5mm diameter in the non-conductive mask layer) shows a $> 50\%$ increase in current density at the edge of the pattern. The simulated current distribution is shown in Figure 4.5. Since the etch

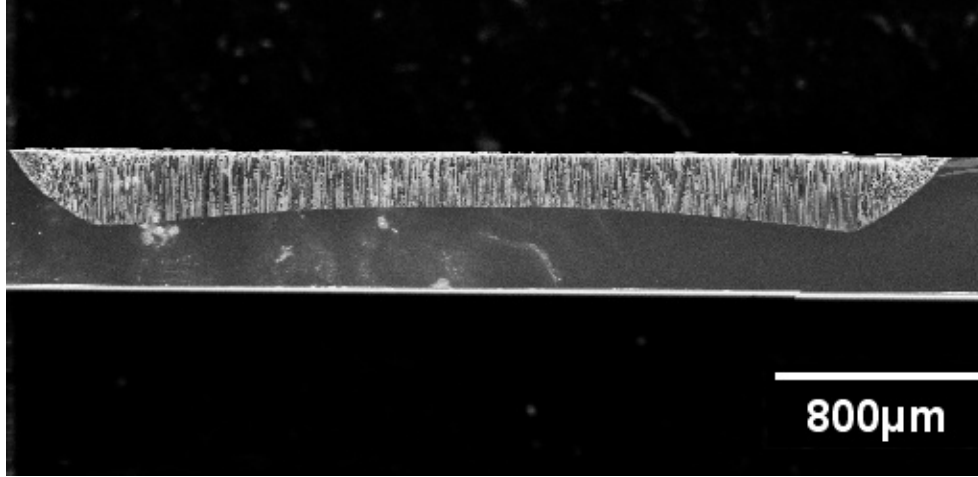


Figure 4.6: SEM image of a p -type silicon sample ($12\Omega\text{cm}$) anodized in organic electrolyte (DMSO:HF=4:1) at $11\text{mA}/\text{cm}^2$ for 6 hours, showing the non-uniform macro PS layer

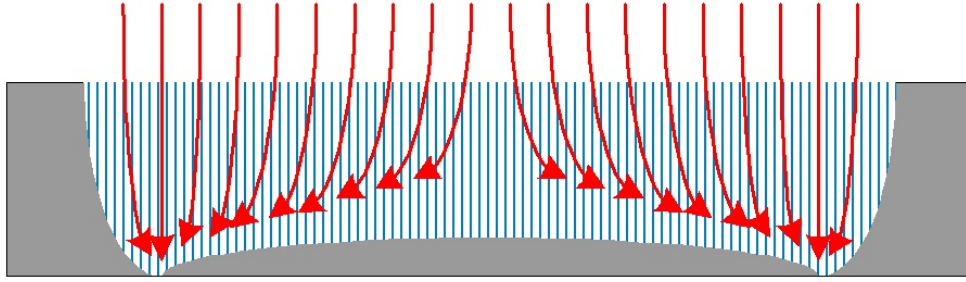
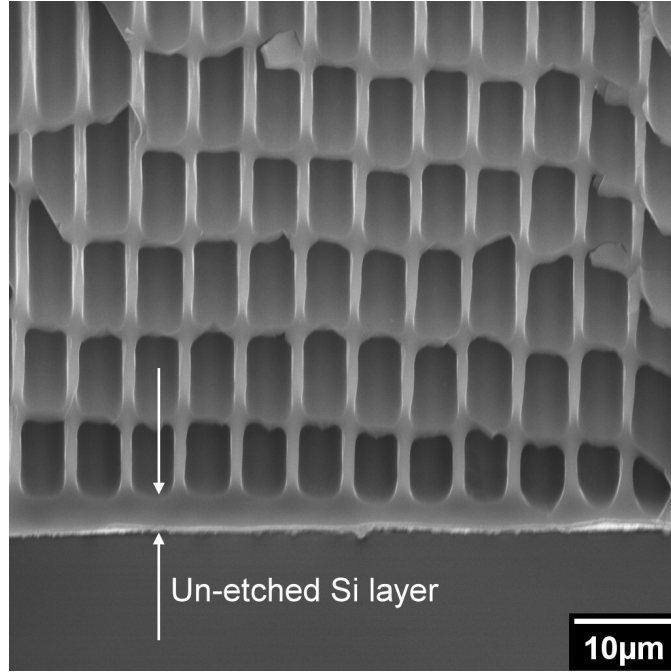


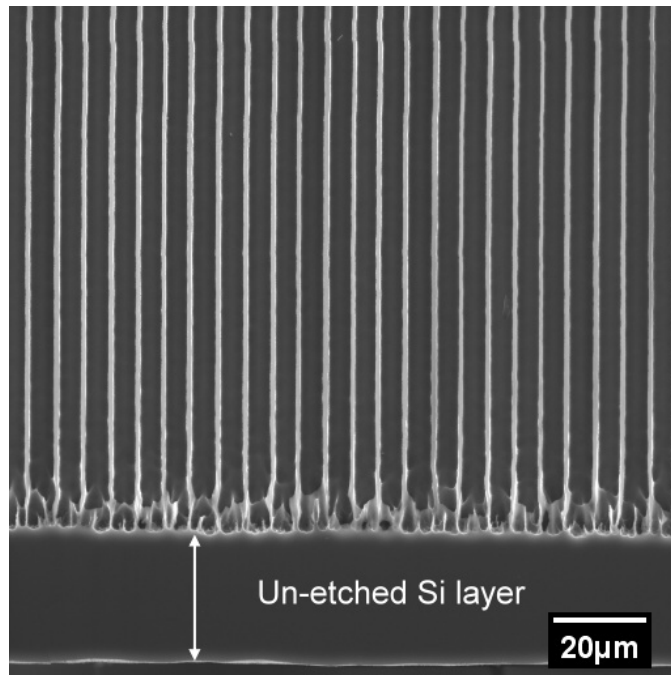
Figure 4.7: Schematic drawing illustrating the formation of the “short circuit” in through wafer etching process

rate of porous silicon is closely related with the current density, any non-uniformity in current distribution will be faithfully reflected in the etching profile. A typical macro porous silicon profile obtained in the lightly doped p -type silicon substrate is shown in Figure 4.6

This non-uniformity won't disappear even we try to form porous silicon through the whole thickness of the substrate. As illustrated in Figure 4.7, when the pores at the edge reach the bottom side of the sample, they will start acting as “short circuits” and conduct most of the etching current through it. Consequently, the pores in the middle lose the driving force (current) and stop growing. Even after extended etch



(a)



(b)

Figure 4.8: SEM images of a *p*-type silicon sample ($17\text{--}23\Omega\text{cm}$) after extended anodization process ($\text{HF:ethonal:H}_2\text{O}=1:2:3$, $27\text{mA}/\text{cm}^2$ for 15 hours). (a) At the edge of the PS region, only a very thin layer of crystalline silicon was left, forming “short circuits”. (b) At the center of the PS region, a relatively thick crystalline silicon layer was left. The rounded pore tips indicate a loss in the “driving force” (current) toward the end of the anodization process.

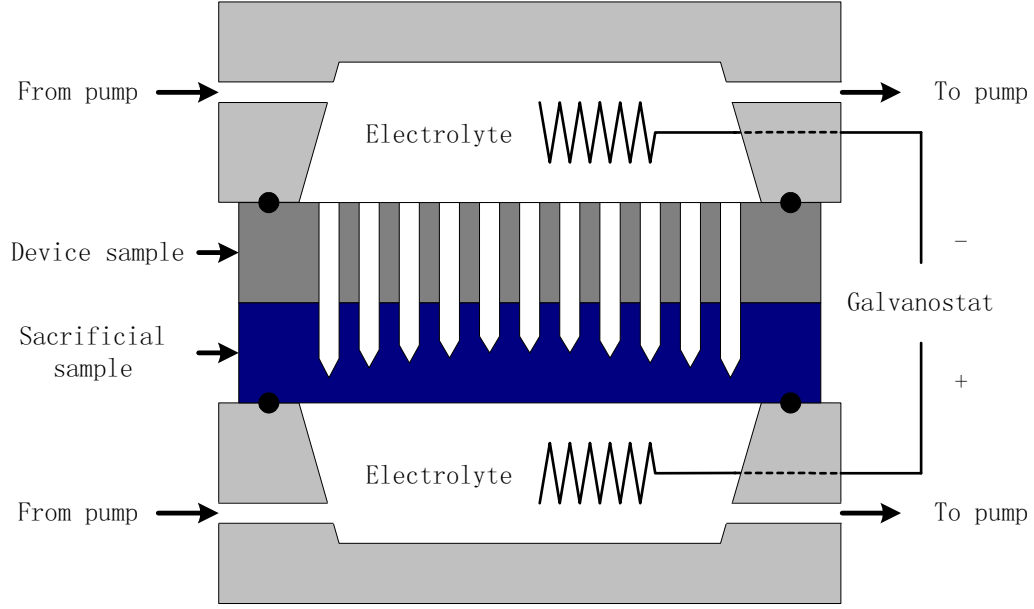
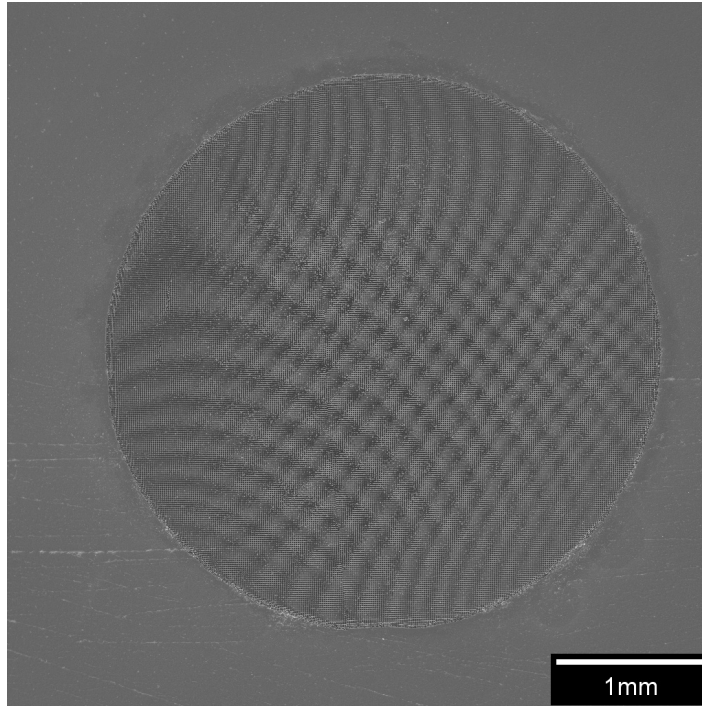


Figure 4.9: Schematic drawing of the setup for the single step etching process for macroporous membrane formation

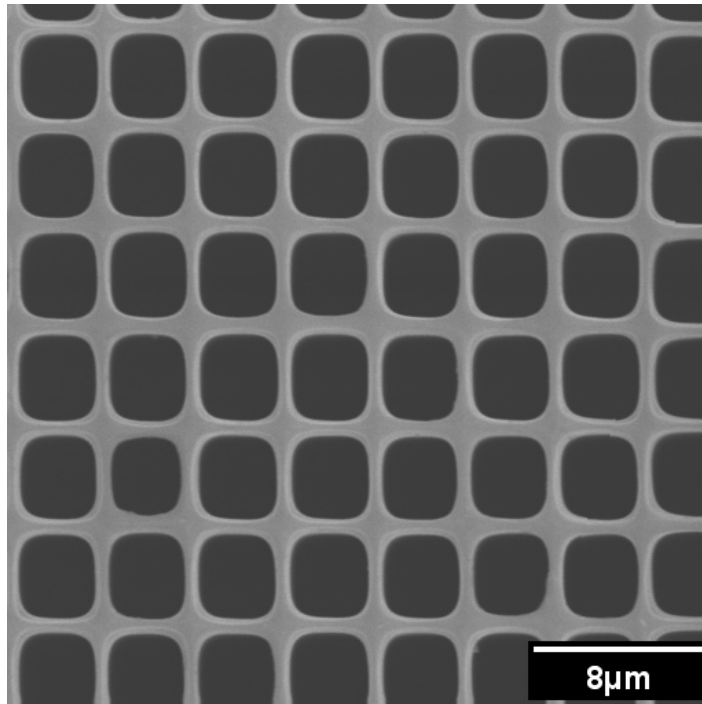
time, the single crystal Si layer in the middle of the pattern still will be much thicker than that on the edge. Figure 4.8 (a) and (b) show the un-etched single crystalline Si layer at the edge and the center of the PS region respectively.

In order to solve the non-uniform etching problem and to avoid additional etch steps required to open the ends of macro pores, a single step etching process for membrane formation has been developed. The setup is shown in Figure 4.9. A sacrificial sample was placed into intimate contact with the backside of the device sample. Given enough etching time, the macro pores in this case will grow beyond the interface between the device sample and the sacrificial sample and all the non-uniformity will be absorbed by the sacrificial sample. A homogeneous porous silicon membrane, therefore, can be formed in a single step. The bottom side of the porous silicon membrane with openings of the through pores is shown in Figure 4.10.

Although the single step etching process works very well for forming porous silicon membrane at sample scale, it has two limitations. First, the membrane has to be of the same thickness of the substrate to be in contact with the sacrificial sample at the back



(a)



(b)

Figure 4.10: (a) SEM image of the bottom side of a porous silicon membrane produced by the single step etching process, showing the through pore region. (b) SEM image of the bottom side of a porous silicon membrane produced by the single step etching process, showing the details of the through pores.

side of the membrane. The single step etching process won't work for membranes with a recess behind it. Second, the contact between the device sample and the sacrificial sample has to be very good to trick the anodization process into proceeding beyond the interface. Close attention should be paid to the flatness of the samples or wafers used in this process. Previous processes may produce unbalanced stress and cause the sample/wafer to warp, which will prevent forming intimate contact between the device sample/wafer and the sacrificial sample/wafer. It's relatively easy to obtain a good contact for small samples. As for the whole wafer, however, the single step etching process becomes unreliable.

In order to form porous silicon membranes for a more generalized situation, an RIE based process has been developed to remove the single crystal Si layer at the backside of the PS sample. The process flow is outlined in Figure 4.11. To avoid damaging the porous structure, a layer of $0.15\mu\text{m}$ thick thermal SiO_2 was first formed to protect the walls of the macro pores. The crystalline silicon layer was then etched away from the backside of the sample by reactive ion etching (RIE). After removing the the single crystal Si layer, the RIE will start removing the silicon between pores. Since the RIE process has a very high selectivity between silicon and silicon dioxide, as shown in the previous section, the oxide layer on the pore walls will stay intact, forming a pillar like structure. The oxide pillars will appear first in the edge area, where the un-etched single crystal Si layer is thin. As the RIE continues, the oxide pillars spread toward the the center of the PS region. As shown in Figure 4.12, the oxide pillars are already quite tall at the edge area, while in the center area the oxide pillars have just emerged. The last step of the process is to remove the thermal oxide layer in buffered HF, after which the macro porous membrane is fully released. Although this process requires extra steps for PS membrane formation, it can be reliably performed at wafer scale. It can also be used for membranes that are thinner than the full thickness of the substrate. From a process integrator's point of view,

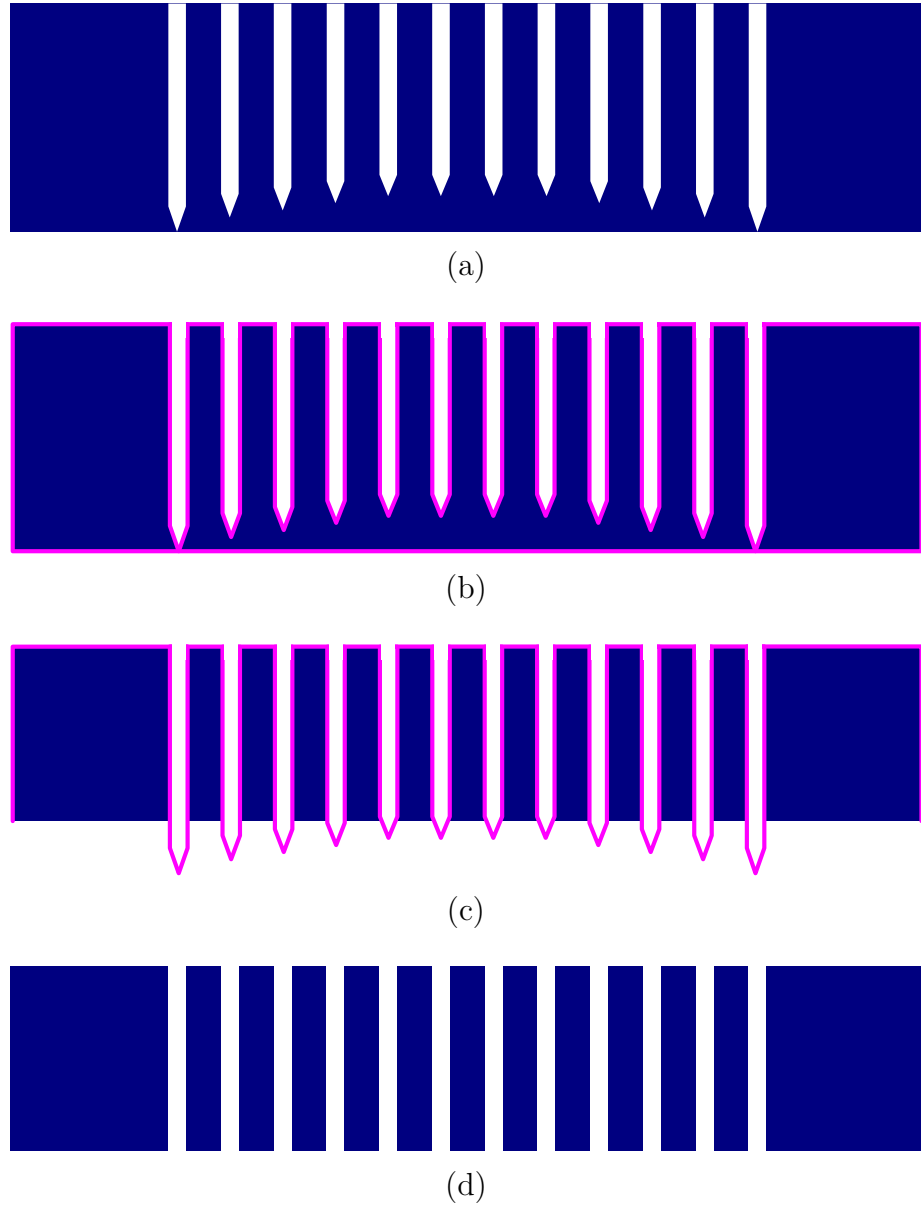
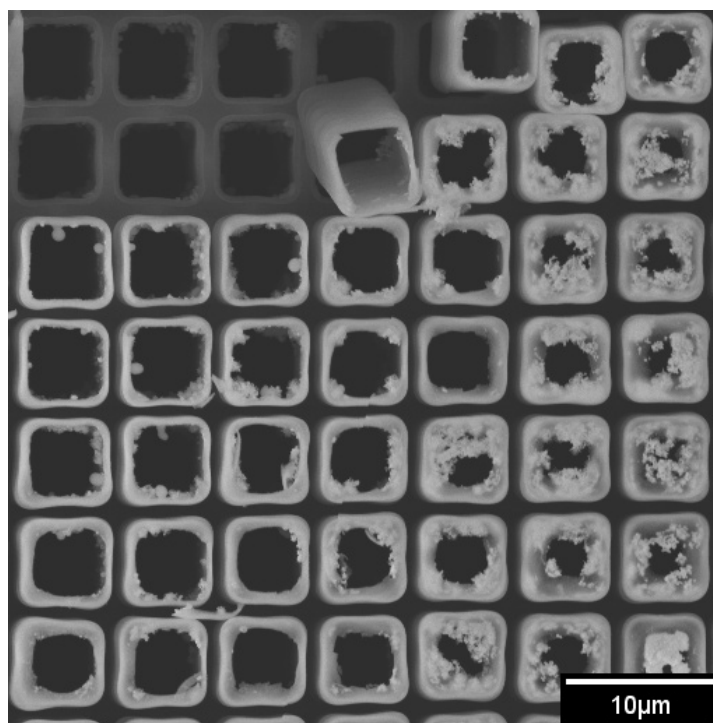
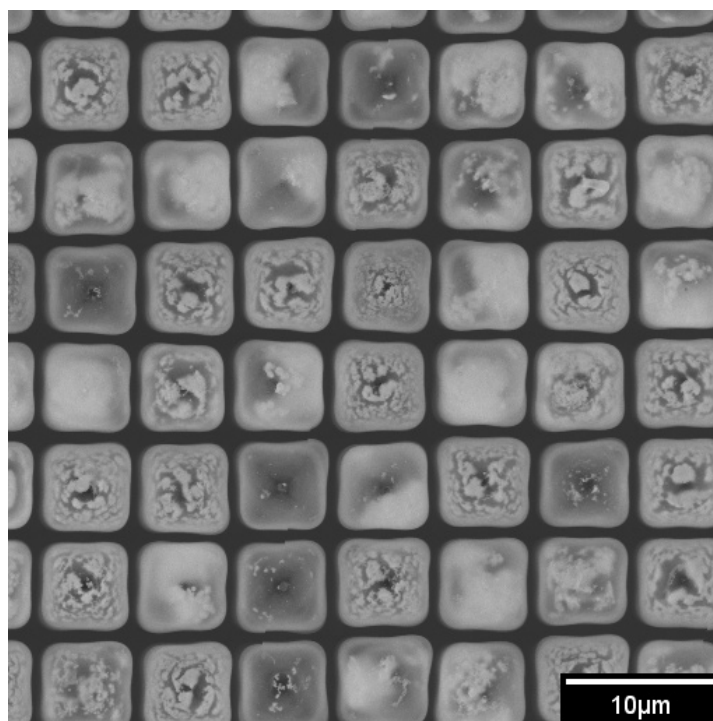


Figure 4.11: process flow used in fabricating macro porous silicon membrane: (a) Macro porous silicon sample with a non-uniform single crystalline silicon layer left; (b) A layer of thermal oxide has been formed to protect the walls of macro pores; (c) The non-uniform single crystalline silicon layer has been removed by RIE, revealing oxide pillars; (d) The macro porous silicon membrane is fully released after removing the oxide layer in BHF.



(a)



(b)

Figure 4.12: SEM images of the back side of a porous silicon sample after RIE etching, showing (a) the edge area with tall oxide pillars, and (b) the center area with emerging oxide pillars.

the availability of both the single step etching process and the RIE based process can provide valuable design flexibility.

4.3 Eutectic Wafer Bonding

One of the many reasons that porous silicon is found appealing in micro system applications is that it can benefit from silicon wafer based bonding processes for device assembly. As we choose the bonding technology for assembling our devices, there are several restrictions though. First, since we don't have any commercial bonder available at MTU, the bonding technology should have a relatively simple and low-cost setup. Secondly, porous silicon sample tends to have a rough surface due to the deterioration of the masking layer in the HF solution. Therefore, the bonding should be able to form a hermetic seal with a minimum requirement on the surface condition. Thirdly, the bonding technology should be able to bond samples of different types, which is often desired to facilitate design flexibility. Finally, the bonding layer should have low out gassing and be compatible with all the chemicals in the work environment of the device. Based on these criteria, eutectic bonding was chosen for porous silicon based device assembly.

4.3.1 Si-Au Eutectic Bonding

Si-Au eutectic bonding is the most widely used eutectic bonding technology. According to the phase diagram shown in Figure 4.13, if silicon and gold are put together, at the eutectic temperature 363°C , 19at.% silicon will diffuse into the gold, forming a eutectic compound. Upon cooling, the eutectic compound will turn into a bond [85]. Although the theory for the Si-Au eutectic bonding looks very simple, the reported practices of the Si-Au bonding vary from a simple hotplate to a state-of-art wafer scale bonder with different bonding layer compositions and the reported results are

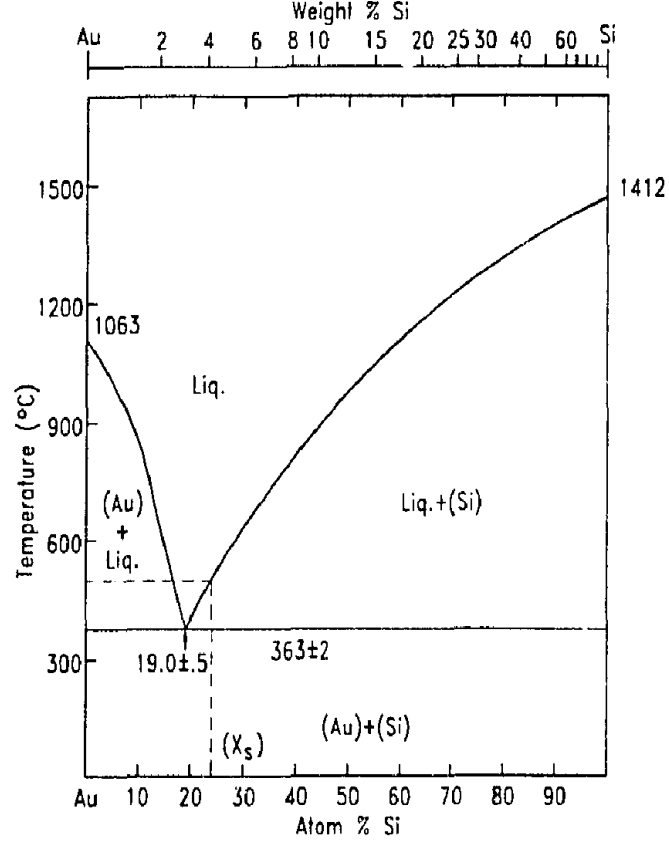


Figure 4.13: Silicon-gold equilibrium phase diagram [85]

poorly reproducible. Based on the available facilities, we decided to start with a hot-plate setup. For initial experiment, diced glass slides with sputtered gold and silicon films were prepared as samples.

In the first set of experiments, a poly silicon and gold stack was sputtered on both pieces of the bonding pair. A gold layer was deposited on the top of the silicon layer to prevent the formation of oxide. The thickness of the silicon and gold layers was adjust to make sure all of the gold would be consumed to form a eutectic between the interfaces of the two samples. Although the gold adheres well on sputtered poly silicon, the diffusion of the gold into the silicon layer totally failed this method. Because gold starts to diffuse into silicon before the eutectic temperature is reached, instead of having an eutectic compound, gold silicide was obtained. No bonding was observed for this set of experiments. It should be noted, that the diffusion of gold

into silicon can also happen during the film deposition. If the sample substrate is not sufficiently cooled, the resulting film will have a very rough surface with dull yellow color instead of a shiny golden surface.

There are two techniques available to avoid the diffusion of gold into the silicon layer. The most obvious one is to separate the gold layer and the silicon layer until the eutectic temperature is reached. This method requires that one of the bonding pieces have only a gold layer and the the other one have only a silicon layer. Then they must be preheated separately until they reach the bonding temperature and be pressed together. Good bonding has been achieved with this sample arrangement on a hotplate at 390°C. But the result was not repeatable due to the oxidation of the silicon layer during the preheating. Even a very thin layer of oxide is sufficient to impede the diffusion of silicon into the gold to form the eutectic compound.

The second method to prevent the gold diffusion is to use a diffusion barrier layer, such as Cr or Ti. However, the existence of the barrier may change the mechanism of the eutectic bond. Temperatures higher than eutectic point were often required to obtain a satisfying bonding [86]. Based on the availability of the materials, Cr was chosen as the diffusion barrier in our experiment. The results of this set of experiments are shown in Table 4.2. The term *partially bonded* means the sample could be separated after the bonding and there were signs of bonding at some, or few, points or regions, while the term *completely bonded* means the sample could not be separated by a wedge and the bonding layer looked uniform. Two conclusions can be drawn from the results of this set of experiments. First, with a Cr diffusion barrier, the bonding temperature for yielding good bonds is much higher than the Si-Au eutectic point (500°C vs. 363°C). Second, for a silicon rich bonding layer, i.e. silicon is over 19at. %, the bonding time is critical to the bonding quality, as shown by the third and forth experiments in Table 4.2. Too long of bonding time will degrade instead of improve the bonding quality. This is because over heating the sample will

Table 4.2: Results of the Si-Au eutectic bonding with Cr as the diffusion barrier

Bonding layer		Temperature (°C)	Time (min)	Result
Piece 1	Piece 2			
Si/Cr/Au(230/100/130 nm)	Si/Cr/Au(230/100/130 nm)	370	5	partially bonded
Si/Cr/Au(230/100/130 nm)	Si/Cr/Au(230/100/130 nm)	455	3	partially bonded
Si/Cr/Au(230/100/130 nm)	Si/Cr/Au(230/100/130 nm)	500	3	completely bonded
Si/Cr/Au(230/100/130 nm)	Si/Cr/Au(230/100/130 nm)	500	5	partially bonded
Si/Cr/Au(230/100/130 nm)	Cr/Au(100/1300 nm)	500	3	completely bonded
Si/Cr/Au(230/100/130 nm)	Cr/Au(100/1300 nm)	500	5	completely bonded

cause excess diffusion of silicon into the gold layer. The excess silicon will form silicon islands in the eutectic compound and prevent the formation of a complete bond [85]. For glass samples, the bonding layer can be adjusted to be Au rich, as in the last two experiments in Table 4.2. With an Au rich bonding layer, the bonding quality is no longer sensitive to the bonding time. This method, however, is not applicable to silicon samples, where there is an “infinite” silicon supply. Given enough bonding time, a silicon sample will make the bonding layer silicon rich anyway.

In order to achieve high quality Si-Au eutectic bonding, there are several points that need to be noted. First, the surface of the bonding samples need to be clean and flat. The existence of particles will create large voids and cause incompleted bonds. Second, the temperature and pressure uniformity across the sample is very critical to the success of the bonding. In our experiment, satisfying bonds were achieved by using a heated soldering iron to heat the top sample and to apply bonding pressure. Replacing the soldering iron with pre-heated weight only yield partial bonds. It is very tricky to bond large samples with the small soldering iron tip. For large samples, a different setup with larger top heating area and uniform applied pressure is required. Bonding between silicon and glass samples has also been attempted. Due to the high bonding temperature and the resulting thermal mismatch between the silicon and glass, the bonded samples were highly stressed. Cracking of the glass sample has been observed during the cooling process or several days after the bonding, which on

the other hand demonstrated the robustness of the bonding layer.

4.3.2 In-Au Bonding

Although Si-Au eutectic bonding has been successfully demonstrated on small samples at MTU, it has been found not appropriate for our applications for three reasons. First, because Si-Au eutectic bonding requires high bonding temperature ($>500^{\circ}\text{C}$) and high pressure that are uniform across the whole sample surface, it is difficult to implement this technology for large samples ($>1\times 1\text{cm}^2$). Commercial bonders or precisely machined fixtures with accurate temperature control and pressure control should be used for repeatable bonding with large samples. Second, the bonding temperature is too high, considering the thermally induced stress. For porous silicon based devices, assembling components of different materials is often required. Since porous silicon samples are relatively fragile, the stress caused by the thermal mismatch can be destructive. A bonding process with lower bonding temperatures would be more desirable. Thirdly, the Si-Au eutectic bonding is not very tolerant. A small non-uniformity in the bonding pressure or a tiny roughness on the surface will result in an incompleted bond. Since porous silicon samples are expected to have a relatively rough surface, a more robust bonding process is desired in this case.

In order to accommodate the rough sample surface, to reduce the thermal stress, and to achieve reliable bonding over a large area with a simple setup, another bonding technique, In-Au bonding, has been tested [87]. Unlike the Si-Au bonding where the eutectic temperature is required for bonding, In-Au bonding can occur below the eutectic temperature. This is due to the extremely low melting temperature of indium. According to the In-Au phase diagram given in Figure 4.14, the melting point of indium is 157°C , which is much lower than the three eutectic points. When the temperature is raised above 157°C , indium will turn into a liquid. With a small amount external pressure, the melted indium can flow around and fill small gaps.

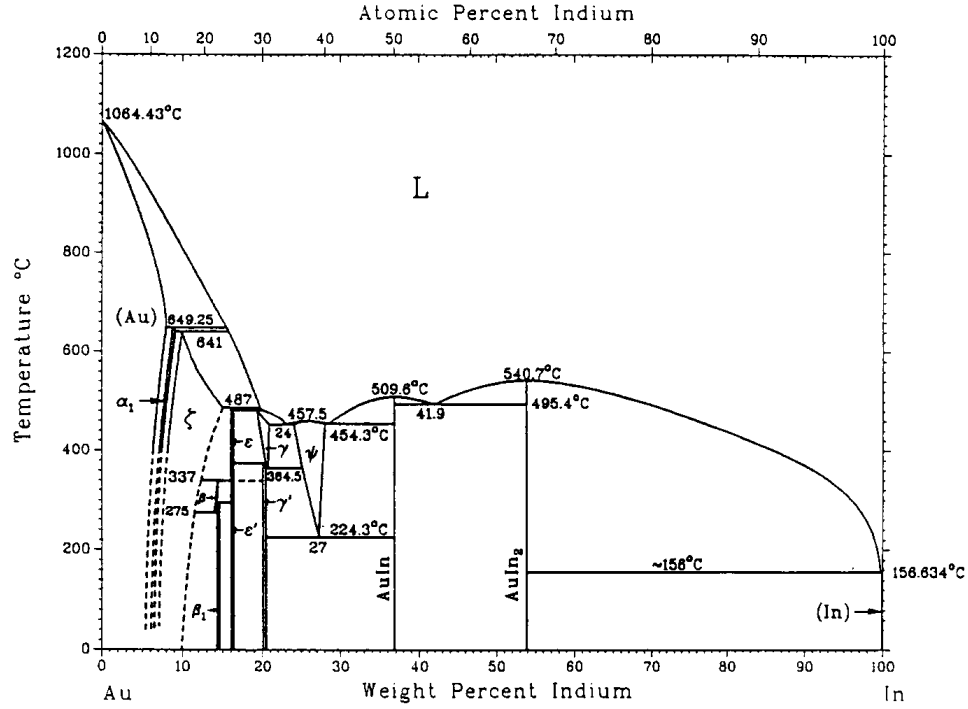


Figure 4.14: Indium-gold equilibrium phase diagram [87]

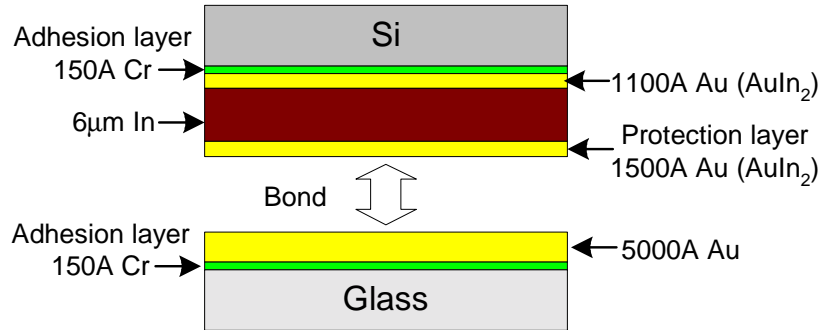


Figure 4.15: Sample preparation for In-Au bonding

Therefore, In-Au bonding not only has a low bonding temperature, but also is less strict about surface conditions.

For In-Au bonding tests, samples were prepared according to Figure 4.15. The films were successively deposited by e-beam evaporation in high vacuums to reduce indium oxidation. Due to the high diffusion rate, AuIn₂ forms almost immediately upon deposition. The Au layer and the subsequently formed AuIn₂ prevent the formation of indium oxide, which will impede the bonding process. A relatively thick

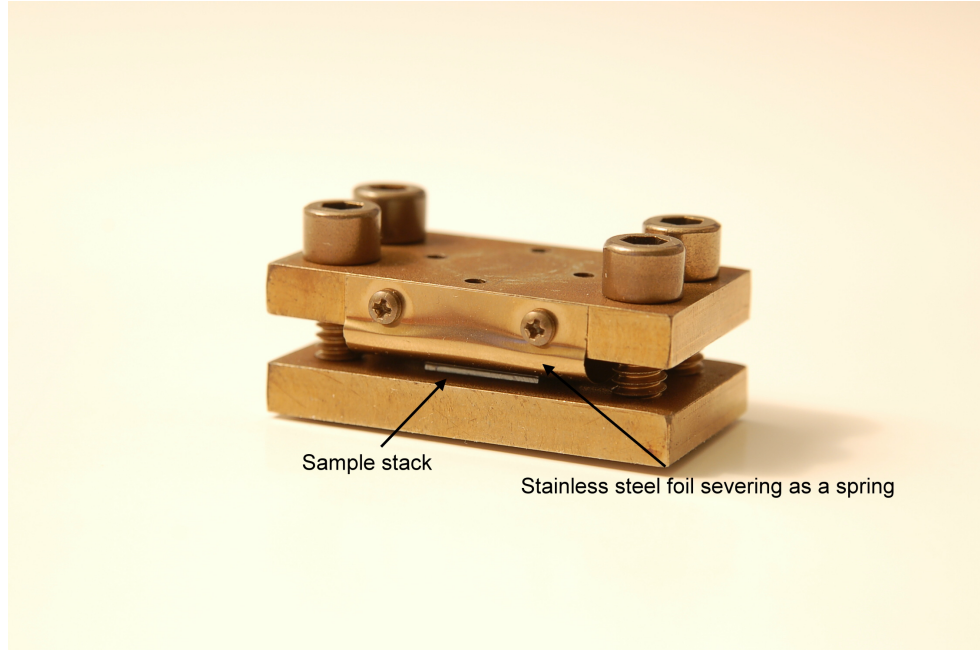


Figure 4.16: Photograph of the fixture for applying uniform pressure on the sample stack during the In-Au bonding

indium layer was used to accommodate surface roughness. The evaporated layers were made in a proportion that is lacking gold to form the In-Au eutectic. Therefore, when the assembly is held at 200°C , indium melts and starts a solid-liquid inter-diffusion at a rate that is several orders of magnitude higher than solid-state diffusion. The liquid indium breaks up the AuIn_2 layer to form a mixture of liquid and solid. The mixture wets and dissolves the gold layer, then forms more AuIn_2 . This solid-liquid inter-diffusion continues until the mixture solidifies, which makes the alloy close to the total composition of the joined layers.

In our experiment, the two samples were held together by a home made fixture, as shown in Figure 4.16. A bended stainless steel shim stock was used as a flat spring to apply a gentle and uniform pressure on the sample stack. The whole assembly was then put into a vacuum oven to minimize oxidation. After the oven reached vacuum, the oven temperature was raised to 200°C and stayed at 200°C for 10min. Afterwards, the heating elements of the oven were turned off and the sample stayed

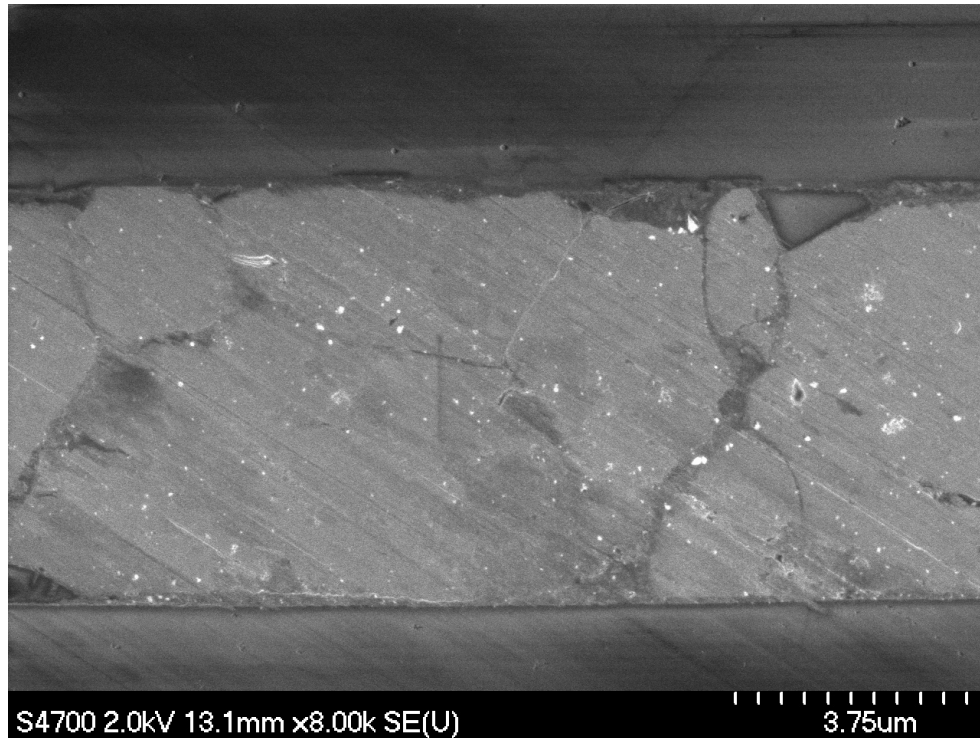


Figure 4.17: SEM photograph of the cross section of the samples bonded by In-Au bonding technology, showing the very thick bonding layer ($>6\mu\text{m}$).

in vacuum before it cooled down to room temperature. Due to the slow cooling rate under vacuum, this process may take several hours. High quality bondings were consistently obtained. The cross section of the In-Au bonding layer is shown in Figure 4.17. The low bonding temperature (200°C) with a very thick bonding layer ($>6\mu\text{m}$) makes In-Au bonding technology ideal for forming hermetic seals on the rough surfaces of PS samples.

Chapter 5

Integrated Calibration Vapor Source

Two generations of micro vapor sources have been developed for calibrating micro gas chromatograph (μ GC) systems. Porous silicon materials were used as a reservoir in the first generation design and a wick in the second generation design. Details about the PS based micro vapor sources, including device design, fabrication flow, and device test, are reported in this chapter.

5.1 First Generation of Source

The first generation of the calibration vapor source was a result of a jointed effort of researchers from MTU, Sandia National Laboratory, and the University of Michigan [88]. The schematic of the device is shown in Figure 5.1. It is a three-layer structure consisting of a top Si layer with a porous silicon reservoir, a Pyrex spacer with a machined aperture, and a base Si layer with diffusion channel and outlet port.

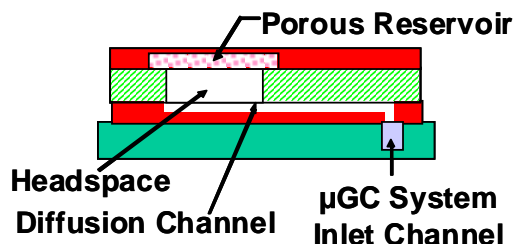


Figure 5.1: Diagram of the integrated diffusion calibration source with porous silicon reservoir [88].

This design allows surface-mounting of the device onto a fluidic substrate upstream from the μ GC preconcentration and separation stages, providing an easy approach to integrate the vapor source into the μ GC. In operation, the porous silicon reservoir is filled with calibrant liquid. Due to the large capillary force that exists in the porous structure, the calibrant liquid is immobilized in the porous reservoir, where it is vaporized into the headspace and then transported through the attached diffusion channel into the sample inlet channel of the μ GC. Two equations can be used to describe the whole process. The first one is the Kelvin equation, which gives the vapor pressure P_v of the calibrant liquid held by a porous medium:

$$\ln\left(\frac{P_v}{P_{sat}}\right) = \frac{2\gamma V_l}{RT r} \quad (5.1)$$

where P_{sat} is the saturation vapor pressure, γ is the surface tension of the liquid, V_l is the molar volume of the liquid, R is the molar gas constant, T is the absolute temperature and r is the liquid radius of curvature. For the liquid held by capillary force, r approximates to the radius of the pore size. The second equation is the diffusion equation, which describes the transportation of the calibrant vapor from the headspace cavity into the sample inlet of the μ GC through the diffusion channel. The calibration source's generation rate q_d can be calculated according to the diffusion equation:

$$q_d = DMPA \ln\left(\frac{P}{P - P_v}\right) / LRT \quad (5.2)$$

where D is the vapor diffusion coefficient, M is the vapor molecular weight, A is the diffusion channel cross section, P is the atmospheric pressure, and L is the diffusion channel length. At constant atmospheric pressure, the generation rate of the calibration source can be adjusted by changing the diffusion channel's dimension or the device's operation temperature. The dimensions of the diffusion channel in this vapor source are designed to provide the required calibration concentration based on the

source calibrant material and operating temperature.

5.1.1 Device Fabrication

MEMS technology has been used to fabricate the calibration vapor source. The layout for the three layers are shown in Figure 5.2. The Pyrex spacer and the bottom silicon layer were fabricated at the Sandia National Lab. The aperture in the Pyrex spacer was produced by ultrasonic machining while the groove for the diffusion channel and the through hole for the outlet port were etched into the bottom silicon layer by deep reactive ion etching. The Pyrex spacer and the bottom silicon layer were then anodically bonded together to form the diffusion channel. The resulting diffusion channel has a cross sectional area of $\sim 0.04\text{mm}^2$. By connecting the diffusion channel to the headspace cavity at different locations, diffusion channels of three different lengths (7.5mm, 13.5mm, and 20.5mm) have been produced. Initial reservoir devices were made from heavily doped *n*-type Si via a standard anodization procedure at Sandia. The resulting meso PS layers (Meso-PS) has a thickness of $\sim 180\mu\text{m}$ and a broad pore size distribution ranging from 5–200nm in diameter, as shown in Figure 5.3.

According to Equation 5.1, the partial pressure of the calibrant vapor P_v in the headspace cavity is related with the pore size of the porous reservoir. Therefore, the broad pore size distribution in the *n*-type meso porous silicon material and the pore size variation in depth will result in a variation of the vapor pressure over time as the liquid in the reservoir is being depleted. With the goal of maintaining a constant generation rate over extended operating periods, efforts were then started to control the size and distribution of pores in the reservoir. To this end, macro porous silicon reservoirs with straight pores and nearly uniform pore diameters were produced at MTU. Boron doped silicon substrates with (100) crystallographic orientation and resistivity of 17-23 Ωcm were used as the starting materials. Thin layers of SiO_2 ($0.1\mu\text{m}$) and poly Si ($0.2\mu\text{m}$) were then deposited as the etching mask for the PS

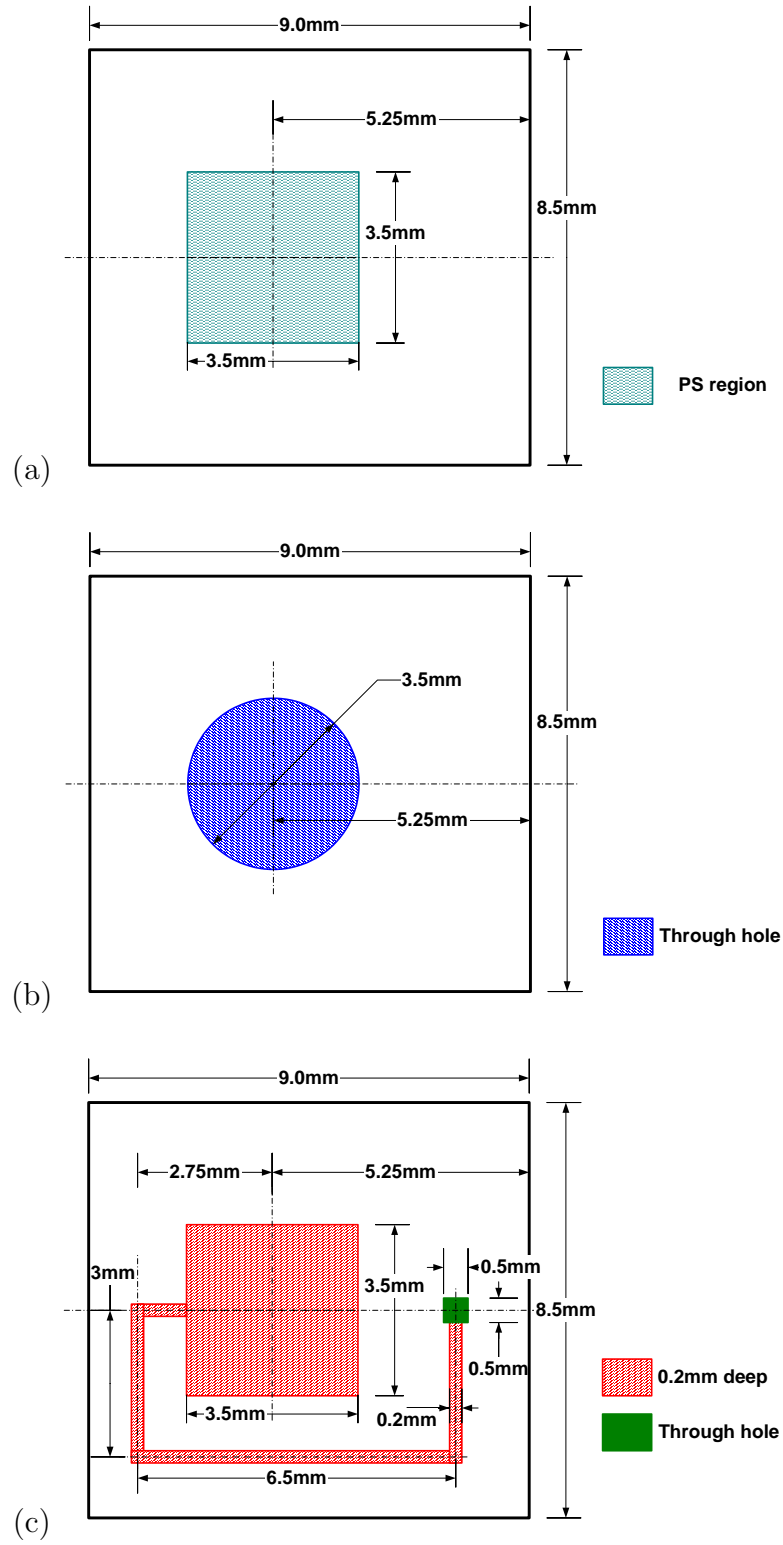
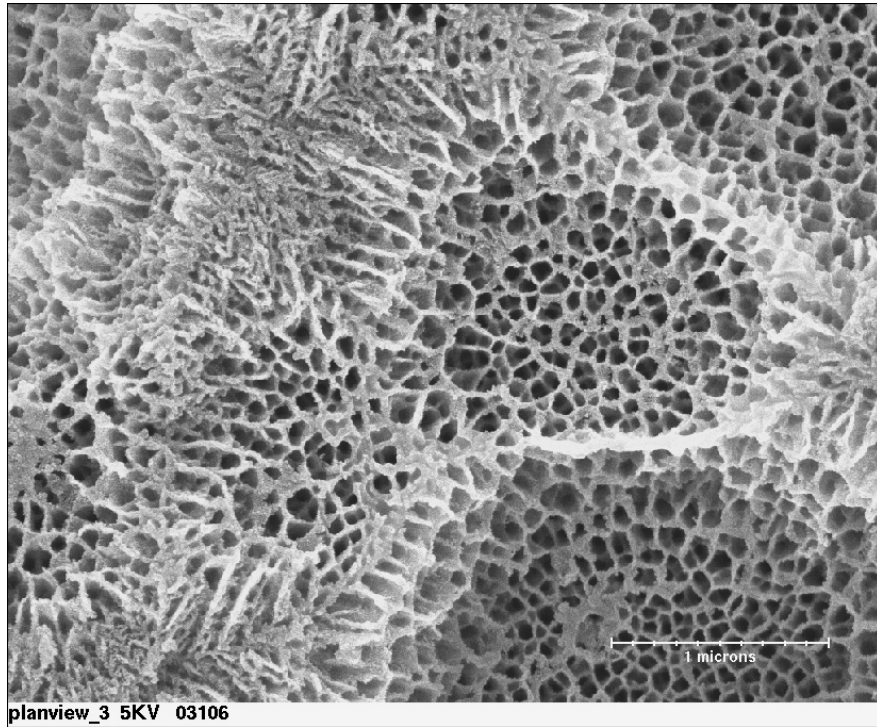
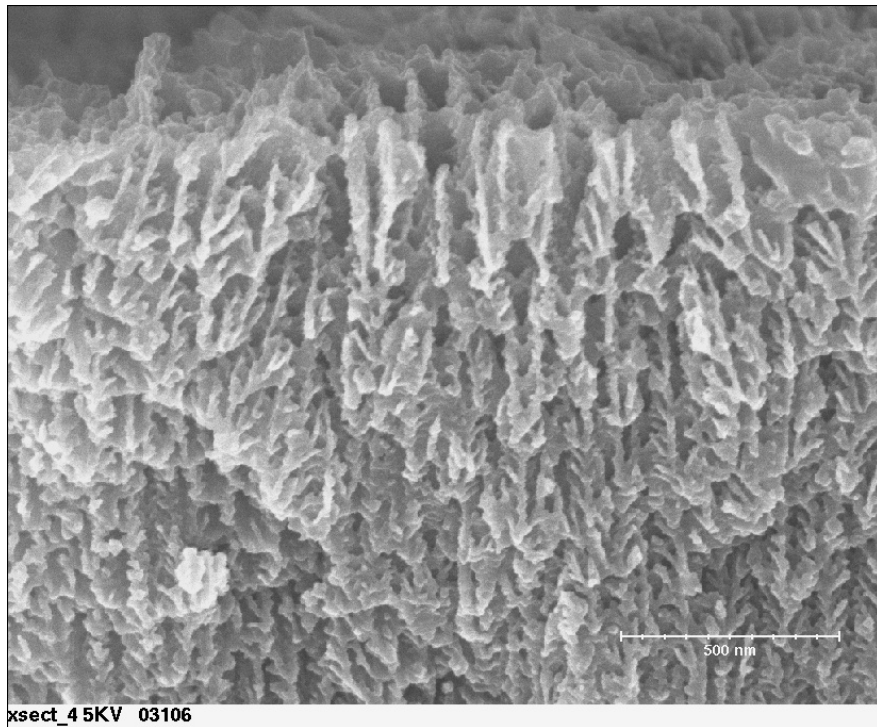


Figure 5.2: Layout of the first generation calibration vapor source. (a) The porous silicon reservoir; (b) The Pyrex spacer with a machined aperture; (c) The bottom silicon layer with diffusion channel and outlet port.



(a)



(b)

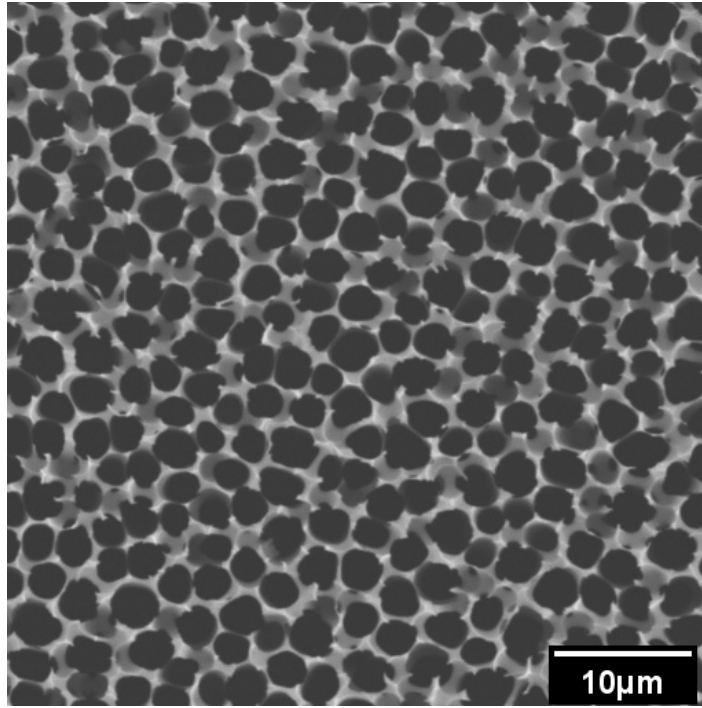
Figure 5.3: SEM images of the *n*-type meso porous silicon produced at Sandia Nation Lab for the calibration vapor source: (a) the top view, (b) the cross sectional view.

formation by RF sputtering. In order to improve the quality of the mask stack, the wafer was then annealed by an RTA at 900C° for 90 seconds. In the subsequent step, the porous silicon region was defined by patterning the masking layers with a combination of dry etching and wet etching, as reported in Section 4.1. The sample was then anodized in a single-tank etching cell with an aqueous electrolyte consisting of cetyltrimethylammonium chloride (CTAC) at 10⁻³M, and HF (49%), ethanol, and H₂O at a volume ratio of 1:1:1. A current density of 85mA/cm² was used. The anodization process lasted for two hours. Figure 5.4 illustrates the uniformity of the etched pores over the entire 280μm depth of the sample. The average pore diameter is 3±0.6μm (Macro-PS).

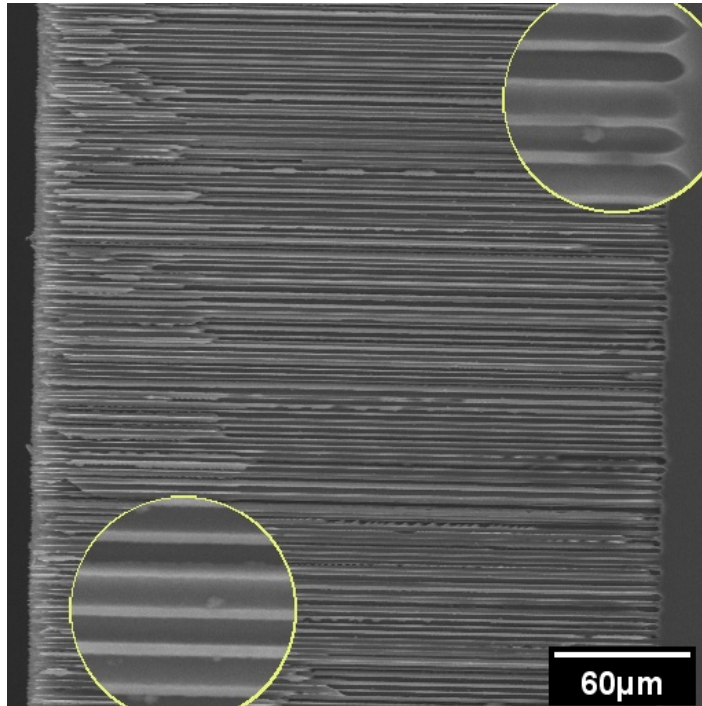
The final fabrication step is to fill the porous silicon reservoir with calibrant liquid and attach it to the diffusion-channel/headspace subassembly. Due to the presence of the calibrant liquid in the reservoir, normal wafer bonding technologies that require thermal treatment can not be used in this case. Instead, VHBTM tapes were used to complete the calibration vapor source assembly. The component parts and an assembled μGC source are shown in Figure 5.5.

5.1.2 Device Test

For testing, n-decane was used as the calibrant liquid. The assembled vapor source was connected to a standard GC-FID (Flame Ionization Detector) through a custom-built polyetheretherketone (PEEKTM) fixture. The experimental setup is shown in Figure 5.6. Results are presented for sources with Meso-PS reservoirs and sources with Macro-PS reservoirs. In all cases, at least 2 hours was required to achieve steady-state, presumably due to off-gassing of vapor adsorbed to the block walls during storage. Figure 5.7 shows the generation rates over time at 25°C. The steady-state generation rate of the source with a Macro-PS reservoir is 0.199 ng/sec, which is within 5% of the theoretical value of 0.189ng/sec. The generation rate for the calibration source with a



(a)



(b)

Figure 5.4: SEM images of a 280μm *p*-type macro porous silicon (2-hour etch at 85mA/cm²): (a) the top view, (b) the cross sectional view.

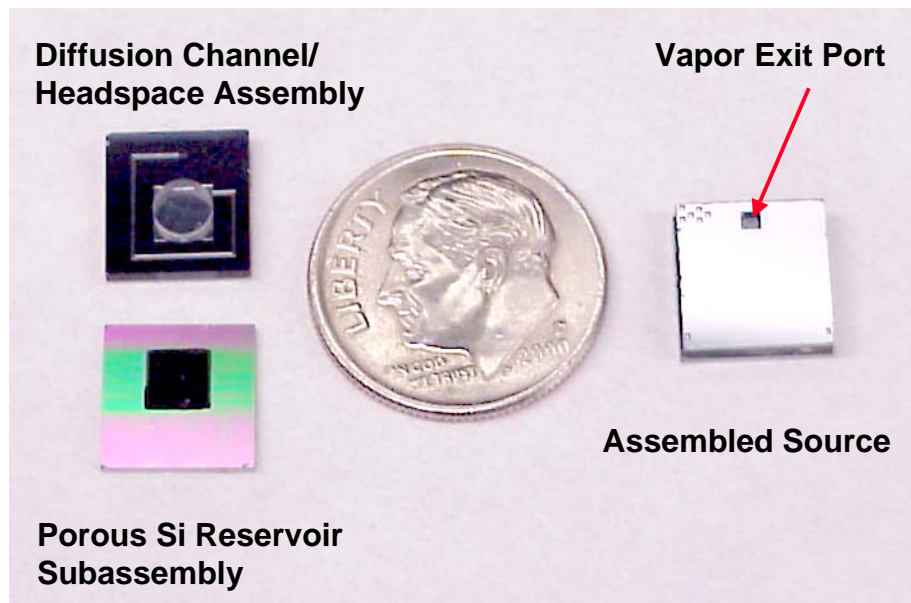


Figure 5.5: The first generation MEMS calibration vapor source before and after assembly.

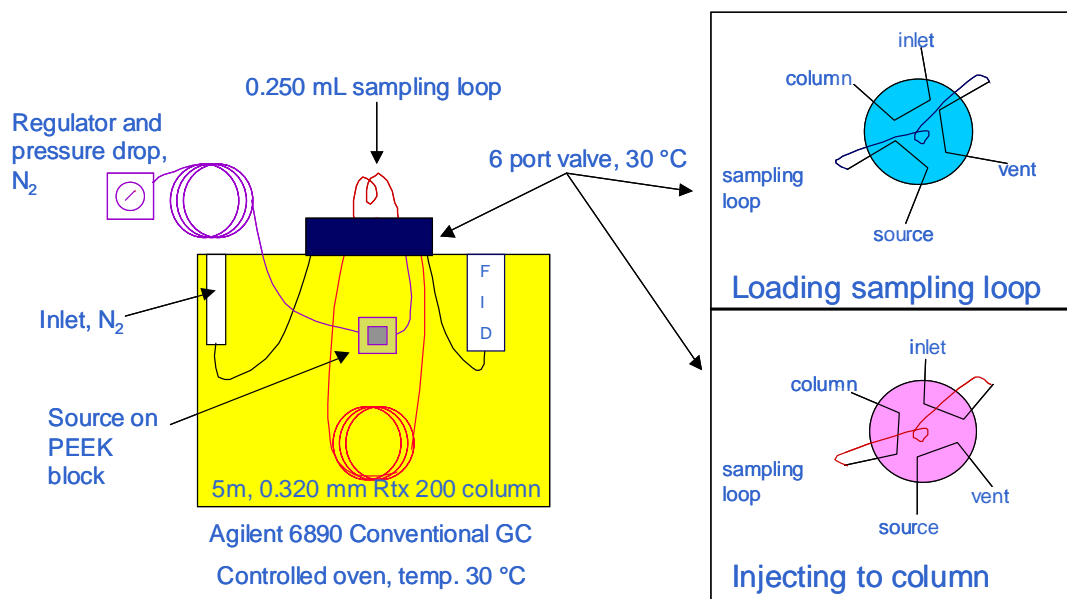


Figure 5.6: Experimental setup for testing the calibration vapor source.

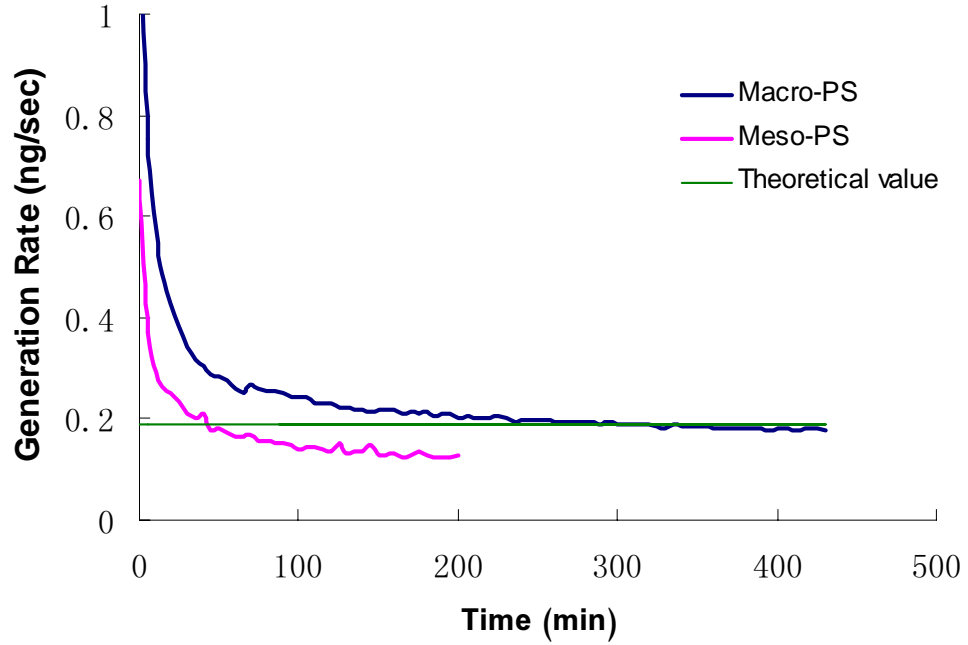
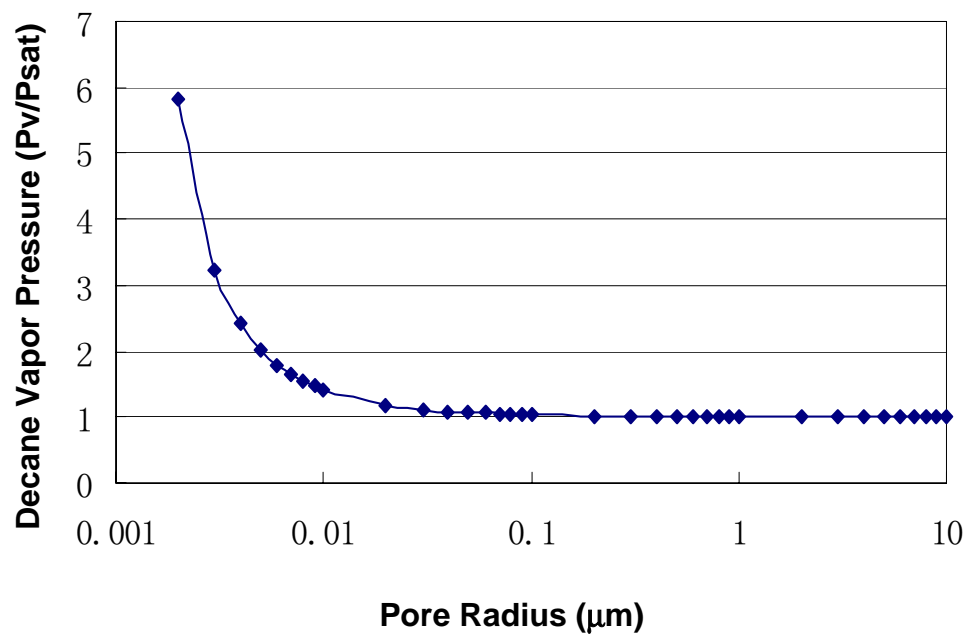


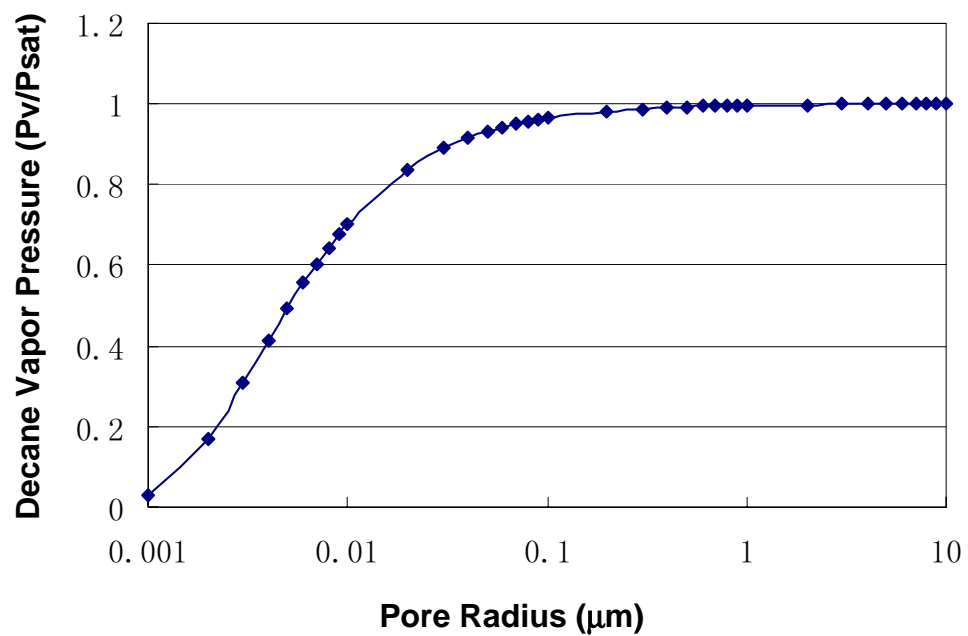
Figure 5.7: Generation rates from the first generation calibration vapor sources at 25°C. Theoretical generation rate is 0.189ng/sec.

Meso-PS reservoir, however, is about 30% lower and has more variations. This is due to the vapor-pressure depression of n-decane in the Meso-PS reservoir, as predicated by the Kelvin Equation (Equation 5.1). The impact of pore sizes on n-decane vapor pressure is shown in Figure 5.8. The Meso-PS has pore sizes in the 5-200nm range, where surface-tension induced vapor-pressure depression is significant. Also, in this pore size range a small variation in pore size will result in a significant variation in the vapor pressure. Therefore, the variations in pore sizes become a major source of the variation in the generation rate for the calibration source with a Meso-PS reservoir. As the pore size increases, the impact of pore size on the vapor pressure reduces. The Macro-PS, for example, has pore sizes around 3.5 μ m, where the vapor-pressure depression is not pronounced any more.

Accelerated aging tests have also been performed to collect information about the device's lifetime. Results show that for a Macro-PS reservoir the generation rate



(a)



(b)

Figure 5.8: Impact of pore size on the vapor pressure with (a) convex liquid surface, and (b) concave liquid surface.

declined over time but stayed within 10% of the initial rate for 31 days at 25°C. The source lifetime (90% depletion) is over one year (389 days) at this temperature. Day-to-day reproducibility was measured at $\pm 2\%$.

5.2 Second Generation of Source

Although the first generation calibration vapor source can provide controllable vapor generation, its design has two drawbacks. Firstly, because the porous silicon reservoir has to be filled before the device is put together, room temperature polymer-based (VHBTM tape) bonding is the only choice for device assembly. Unfortunately, those polymer-based bonds not only introduce contaminative vapors, but also suffer deterioration in the presence of the calibrant liquid, such as n-decane. Secondly, since the porous silicon reservoir cannot be refilled after assembly, the vapor source's lifetime is limited by the depth of the porous silicon layer and the storage time before utilization. In order to improve the calibration vapor source's manufacturability and to extend its lifetime, a second generation vapor source using a PS wick and an external reservoir was developed.

The new design of the integrated calibration source is shown in Figure 5.9. It

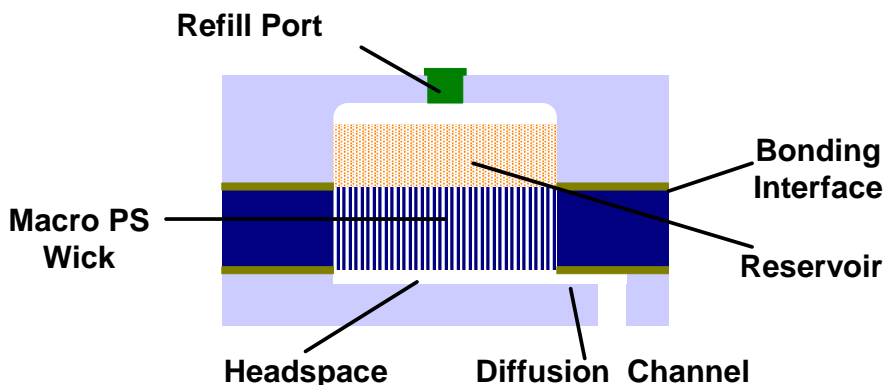


Figure 5.9: Schematic of the integrated calibration source with a macro porous silicon wick.

consists of three layers. The top layer has a deep recess and a through hole, which serve as the reservoir and the filling port of the calibration source. The middle layer is a porous silicon membrane, which serves as a wick for the reservoir. The bottom layer has a shallow recess of the same size of the PS wick, a groove and a small hole in it. When the device is assembled, the shallow recess will form a headspace over the PS wick; the groove will form a diffusion channel; and the small hole becomes an outlet port for the diffusion channel. In operation, the reservoir will be filled with calibrant liquid through the filling port. The PS wick holds the calibrant liquid by capillary forces while allowing the calibrant vapor to enter into the headspace. The calibrant vapor then transports through the attached diffusion channel and the outlet port into the sample inlet of the μ GC, where the calibrant vapor will mix with the carrier gas stream.

Fabrication of the second generation calibration vapor sources has been accomplished at MTU. The layout for the three layers are shown in Figure 5.10. Both the reservoir layer and the diffusion channel layer are made from #7740 Pyrex glass using micromilling [89]. The reservoir has a capacity of $6.7\mu\text{L}$. Diffusion channels of three different lengths (7.5mm, 13.5mm and 20.5mm) and a cross section of $200\times 200\mu\text{m}^2$ have been fabricated. Based on the test results of the first generation vapor sources, macro porous silicon was chosen as the PS wick. To further improve the stability of the generation rate, pre-structuring of the sample surface was used to produce highly ordered macro pore array. The fabrication process for the macro porous silicon wick is outlined in Figure 5.11. *p*-type (100) substrates with resistivity of $17\text{-}23\Omega\text{cm}$ was used as the starting material. In order to form a good electric contact during the anodization process, the backside of the wafer was initially implanted with a high-dose ($\sim 10^{15}\text{cm}^{-2}$ at 80KeV) of boron. The implantation was followed by a rapid thermal annealing (RTA) at 1000°C for 1 minute to activate the dopants. An etching mask stack, consisting of SiO_2 ($0.1\mu\text{m}$), poly Si ($0.2\mu\text{m}$), Si_xN_y ($0.2\mu\text{m}$), was then deposited

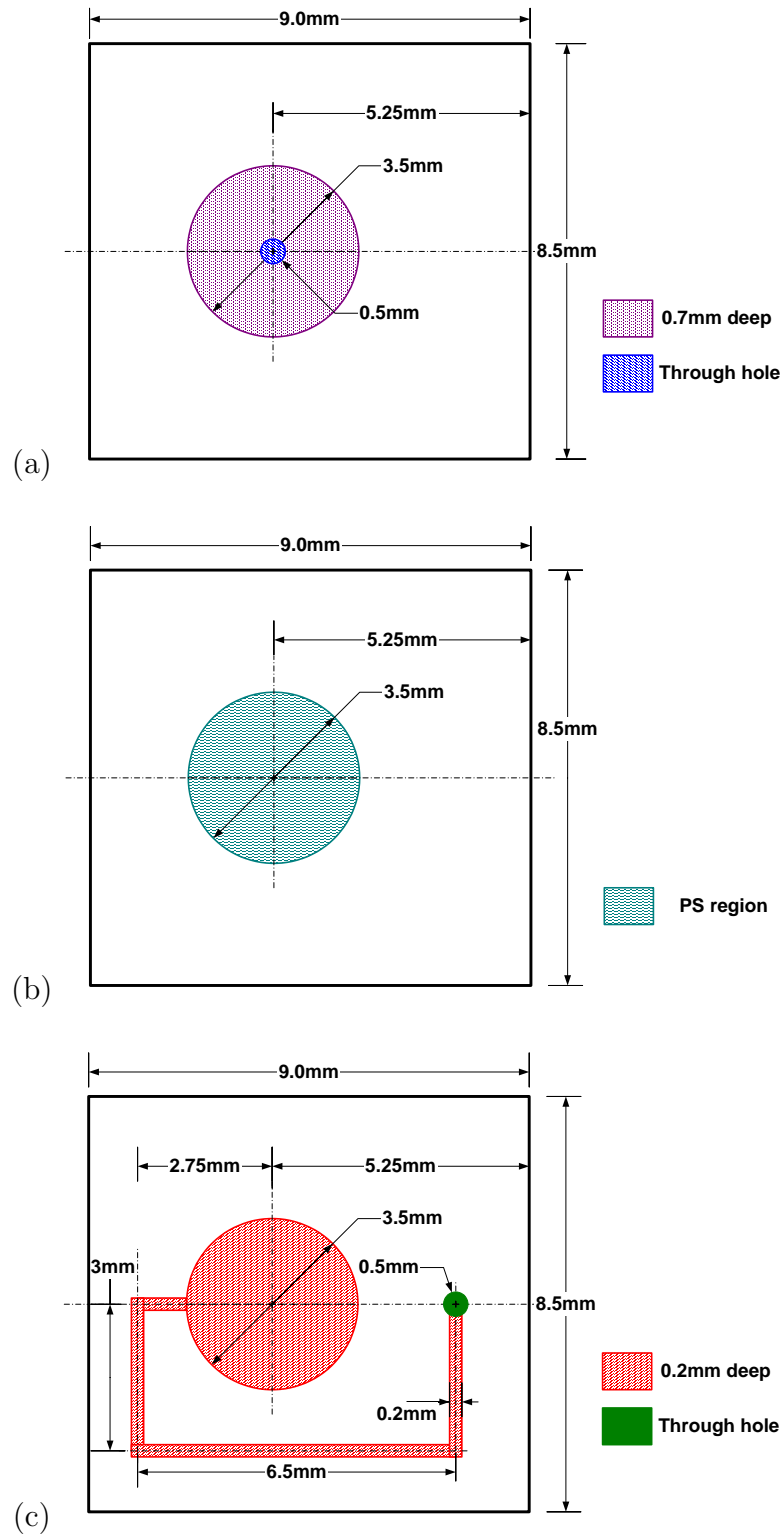


Figure 5.10: Layout of the second generation calibration vapor source. (a) The top Pyrex layer with external reservoir and filling port; (b) The porous silicon wick; (c) The bottom Pyrex layer with diffusion channel and outlet port.

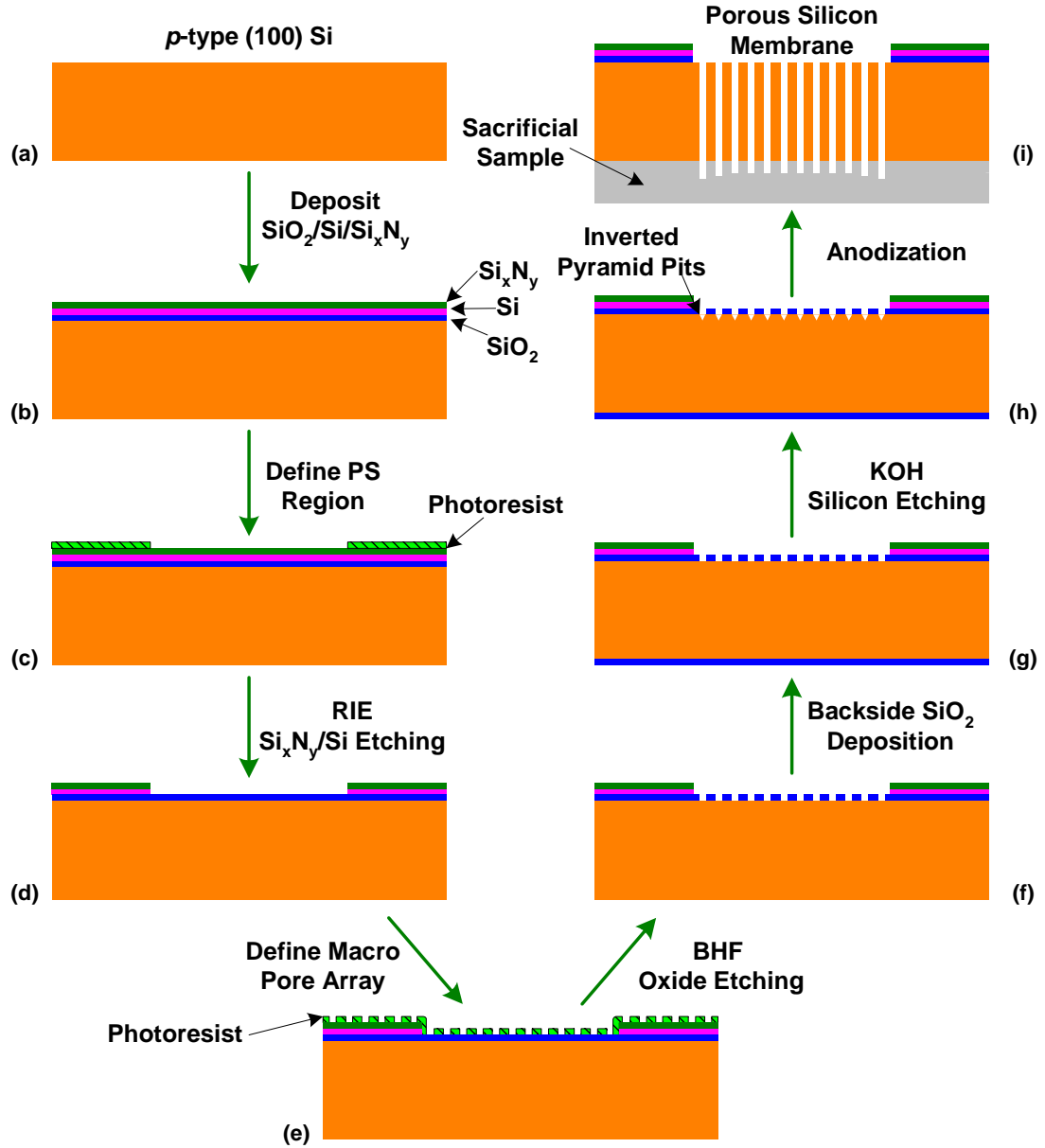


Figure 5.11: Process flow for the macro porous silicon wick: (a) *p*-type (100) silicon substrate with resistivity of 17-23 Ωcm , (b) deposit $\text{SiO}_2/\text{Si}/\text{Si}_x\text{N}_y$ layers as the anodization mask, (c) define the porous silicon region (3.5mm diameter circle) by lithography, (d) transfer the PS region pattern into the $\text{Si}/\text{Si}_x\text{N}_y$ layers by RIE, stopping at the oxide layer, (e) define the macro pore array by lithography, (f) transfer the macro pore array pattern into the oxide layer by BHF etching, (g) deposit SiO_2 on the backside of the sample, (h) form arrays of inverted pyramid pits by KOH etching, (i) form macro porous silicon membrane by anodizing the sample in HF based solution (HF:ethanol: H_2O = 1:2:3, 10^{-3}M CTAC, $27\text{mA}/\text{cm}^2$, 16hrs) with sacrificial sample.

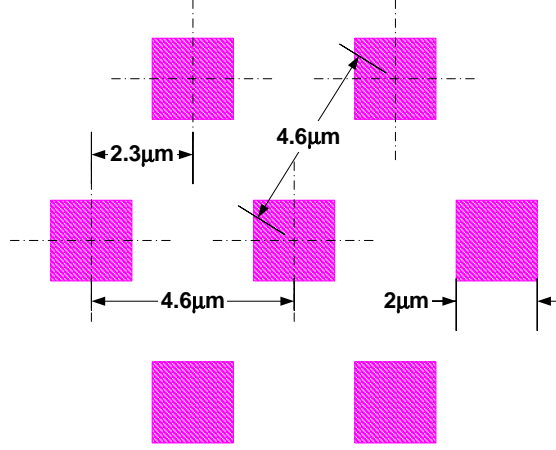
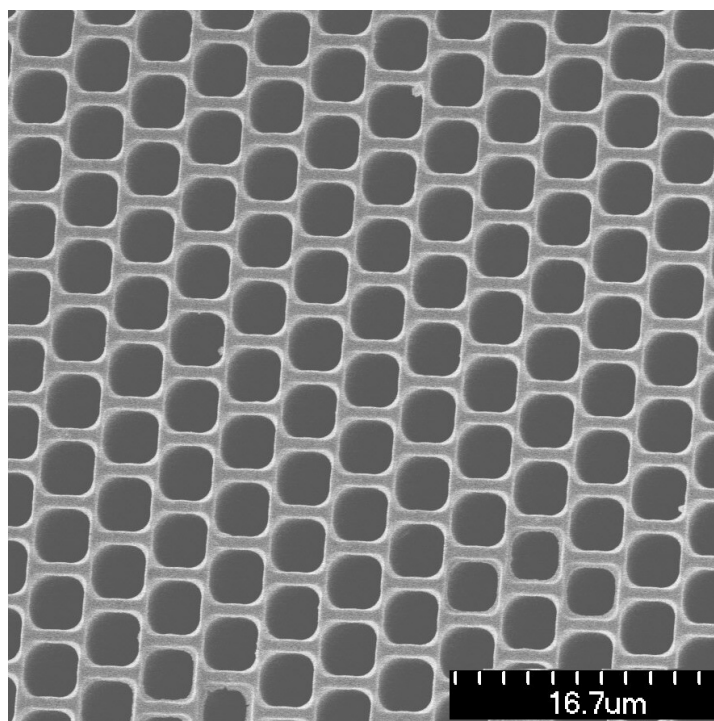


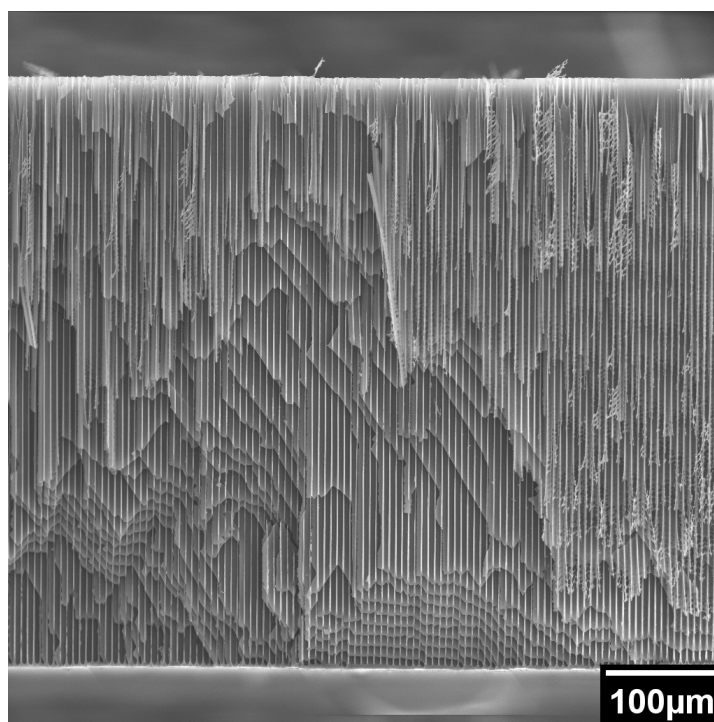
Figure 5.12: Drawing of the macro pore array pattern for the porous silicon wick.

by RF sputtering, followed by an RTA annealing at 800°C for 60 seconds to improve the quality of the mask stack. Standard photolithography was used to define the PS region (circular with a diameter of 3.5mm). After patterning the photoresist, RIE etching was used to transfer the pattern into the nitride and the poly silicon layers, stopping at the oxide layer. Then a second lithography step was used to define the macro pore array. The pattern of the macro pore array is shown in Figure 5.12. It consists of hexagonally packed pores with unit cell size of $4.6\mu\text{m}$. The array pattern was then transferred into the exposed oxide layer by BHF etching. After protecting the backside of the wafer with a layer of RF sputtered oxide, a KOH etching was used to form arrays of inverted pyramid pits as initial pores.

Macro porous silicon formation was carried out in a double-tank etching cell with an aqueous electrolyte consisting of cetyltrimethylammonium chloride (CTAC) at 10^{-3}M and HF (49%), ethanol, H_2O at volume ratio 1:2:3. The anodization current density was set at $27\text{mA}/\text{cm}^2$. This anodization condition has been optimized to produce very deep macro pores, as reported in Section 3.4.2. Through wafer pores ($>500\mu\text{m}$ long) were obtained by simply stacking a sacrificial sample at the backside of the macro-porous sample during the anodization. Details for the through-wafer pore formation can be found in Section 4.2. The surface and the cross section of



(a)



(b)

Figure 5.13: (a) Top view of the macro porous silicon wick; (b) Cross sectional view of the macro porous silicon wick.

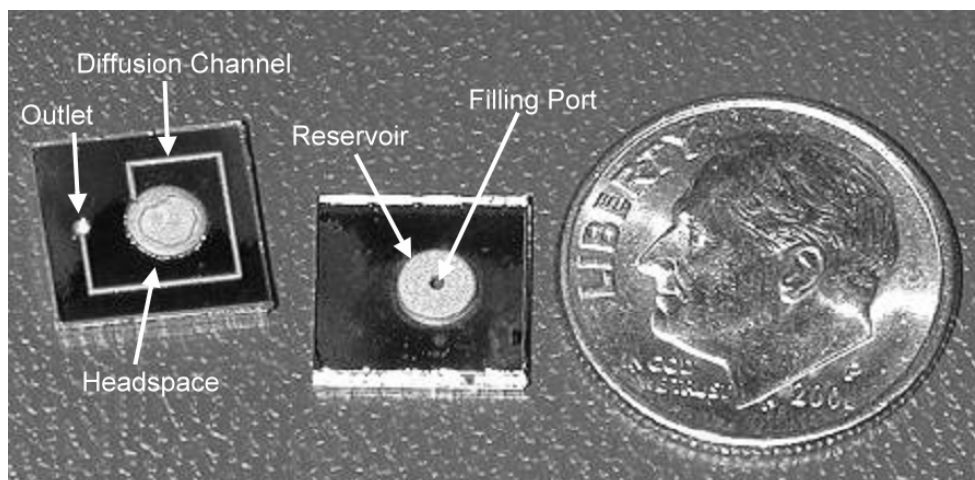


Figure 5.14: Picture of two assembled calibration sources, showing the reservoir, the filling port, the headspace, the diffusion channel, and the outlet port.

the macro porous membrane are shown in Figure 5.13. The three-layer device was then assembled by In-Au bonding, which provides a uniform hermetic seal without introducing organic contamination. The conditions for the In-Au bonding were given in Section 4.3. The final devices are shown in Figure 5.14.

Testing of the new calibration source was carried out by researchers at the University of Michigan. Again, the experimental setup shown in Figure 5.6 was used. The source was loaded with n-decane and connected to a standard GC-FID (Flame Ionization Detector) through the custom-built polyetheretherketone (PEEKTM) fixture. Reproducibility of the vapor generation rate has been tested over several weeks at constant temperatures. Small variations of 0.1% over a 9-hour period and 0.5% over a week have been observed, as shown in Figure 5.15. Repeatable results were obtained between refills of the reservoir.

The excellent stability of the vapor generation rate owes much to the macro porous silicon wick. According to Figure 5.8, the macro pores ($3.5\mu\text{m}$) fall in the range where a small pore size variation will not cause significant change in the vapor pressure. Under this condition, the straight pores in the macro PS wick, which have uniform pore size through the full thickness, are able to produce a constant vapor pressure

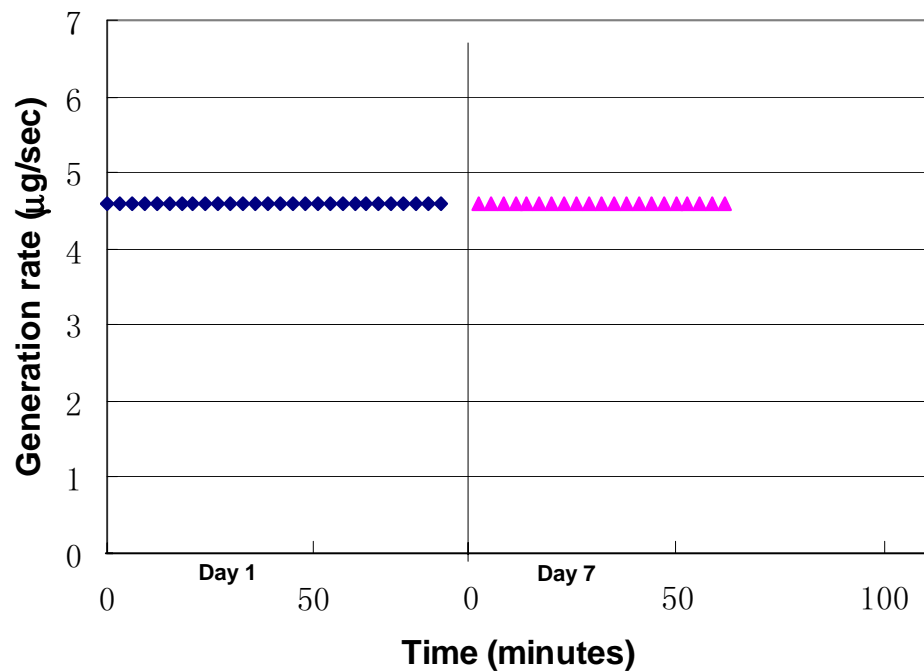


Figure 5.15: Steady-state generation rate of the second generation vapor source at 30°C, showing small variations of 0.1% over a 9-hour period and 0.5% over a week.

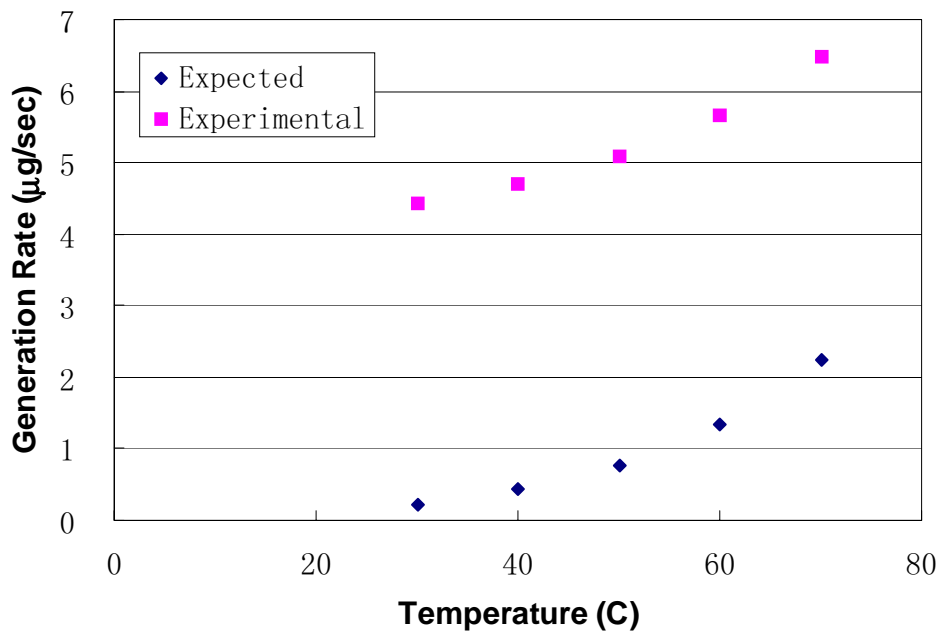


Figure 5.16: Temperature dependence of generation rate for 30–70°C.

when the liquid-gas interface moves in the wick during the operation of the calibration source.

Temperature dependency of the generation rate has been measured as well. The result is shown in Figure 5.16. The experimental data follow the trend predicted by the classic diffusion model. However, the measured generation rates are much higher than the theoretically predicted ones. Since the difference between the two sets of data is almost temperature independent, it is most likely caused by a calibration shift of the FID, but that hypothesis has not yet been experimentally corroborated.

5.3 Conclusions

Two generations of calibration vapor sources have been fabricated and tested. In the first design, controllable vapor generation has been achieved by using a micro machined diffusion device with a porous silicon reservoir. A macro porous silicon reservoir with straight pores has been observed to provide better stability over a meso porous silicon reservoir.

In order to improve the manufacturability of the device and to provide longer lifetime, a second design of the vapor source with a macro porous silicon wick and a micromachined reservoir has been developed. For device assembly, the VHBTM tape was replaced by In-Au bonding, which provides a uniform hermetic seal without introducing organic contamination. By utilizing a macro porous silicon wick with regular pore arrays, vapor generation with excellent stability has been achieved. The source has shown uniform and repeatable vapor generation for n-decane with less than a 0.1% variation in 9 hours, and less than a 0.5% variation in rate over 7 days. Equipped with a refillable reservoir, this vapor source can be used for extended μ GC field deployment.

Chapter 6

Porous Silicon Based Particle Filter

A porous silicon based particle filter has been developed at MTU for the inlet of the μ GC. Important aspects of the PS filter, such as the device design, fabrication, and testing are reported in this chapter. A theoretical model is presented as well to aid the understanding of the filtration mechanisms of the PS material.

6.1 Device Design and Fabrication

The particle filter consists of a porous silicon membrane supported by a bulk silicon frame. Only one mask layer is required to fabricate this structure. The layout is shown in Figure 6.1. The fabrication process for the particle filter is outlined in Figure 6.2. Based on the knowledge of filtration mechanisms, macro porous silicon with a tortuous pore path was chosen as the porous media for the particle filter. The starting material for producing this type of material is *p*-type (111) substrates with resistivity of 10-20 Ω cm. The first step was to deposit thin layers of SiO₂ (0.1 μ m) and poly Si (0.2 μ m) as the etching mask for the PS formation. In order to improve the quality of the mask stack, the wafer was then annealed by an RTA at 900C° for 90 seconds. In the subsequent step, the porous silicon region was defined by patterning the masking layers with a combination of dry etching and wet etching, as reported in Section 4.1. The same pattern was then transferred to the backside of the wafer to define the membrane region. A subsequent deep reactive ion etching (DRIE) was used on the

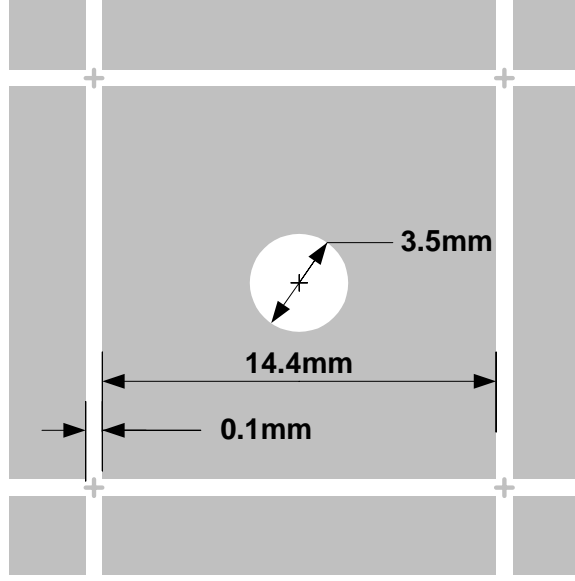


Figure 6.1: Layout of the first generation porous silicon based particle filter, showing the die, the circular membrane region, and gaps for scribing.

backside of the sample to form a silicon diaphragm. In order to simplify the backside contact issue, the anodization process was carried out in a double-tank etching cell for 6 hours. A current density of $15\text{mA}/\text{cm}^2$ and a dimethylsulfoxide-based electrolyte (9.5wt% HF) were used in the anodization process. This PS formation condition has been optimized to generate macro pores with tortuous paths, as reported in Section 3.5. Due to the non-uniform current distribution and bottom side passivation, even after an extended duration of anodization, the resulting PS layer still has a donut shaped profile with a single crystalline silicon layer of non-uniform thickness at the backside of the sample. The RIE based process, as described in Section 4.2, was then used to remove the single crystalline silicon layer. The walls of macro pores were coated with a layer of $0.15\mu\text{m}$ thick thermal SiO_2 before the crystalline silicon layer was etched away from the backside of the sample by reactive ion etching. Since the RIE process has a high selectivity between silicon and silicon dioxide, the oxide layer effectively protected the macro pore structure from being damaged during the RIE process. After removing the thermal oxide in buffered HF, the macro porous membrane of uniform thickness was released. The resulting porous silicon membrane

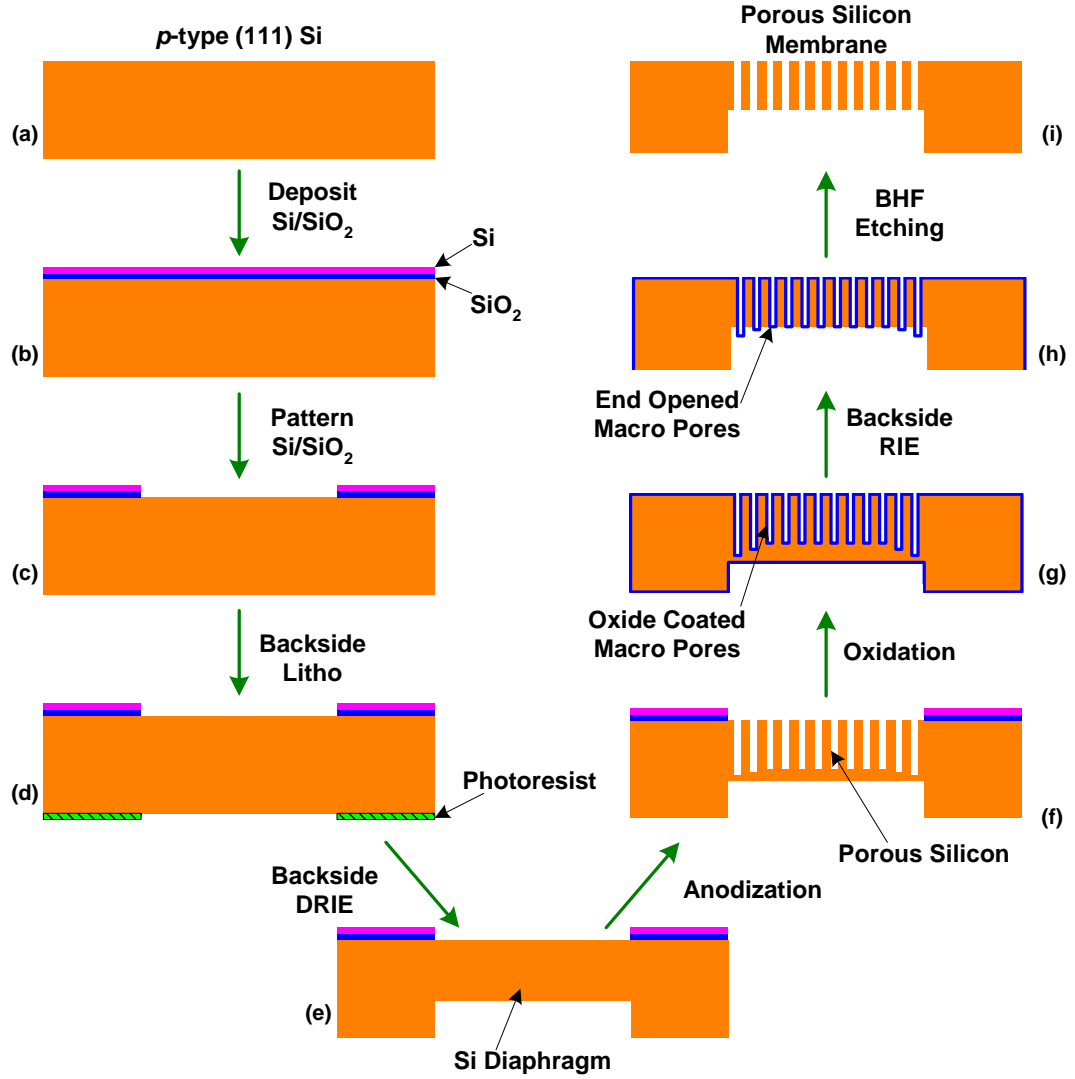


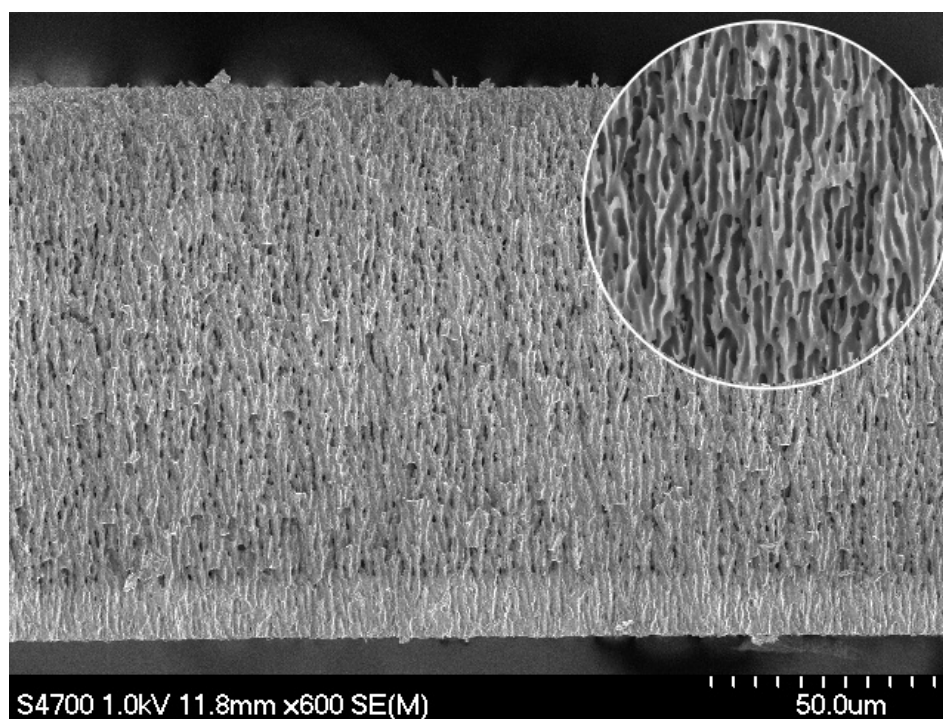
Figure 6.2: Process flow for the porous silicon based particle filter: (a) *p*-type (111) Si substrate with resistivity of 10-20Ωcm, (b) deposition of SiO₂/Si layers as the anodization mask, (c) pattern the SiO₂/Si masking layers to define the PS region, (d) backside litho to define the membrane region, (e) Deep Reactive Ion Etching (DRIE) to form the silicon diaphragm, (f) anodize the silicon diaphragm, (g) coat macro pores with thermal oxide, (h) Reactive Ion Etching (RIE) away the single crystalline silicon layer from the backside of the diaphragm, (i) BHF etching away the thermal oxide layer to release the macro porous silicon membrane

has a diameter of 3.5mm and a thickness of 120 μ m. Figure 6.3 shows the top view and the cross sectional view of the macro porous silicon membrane. The average pore diameter is $\sim 1.5\mu$ m and the porosity is $\sim 60\%$.

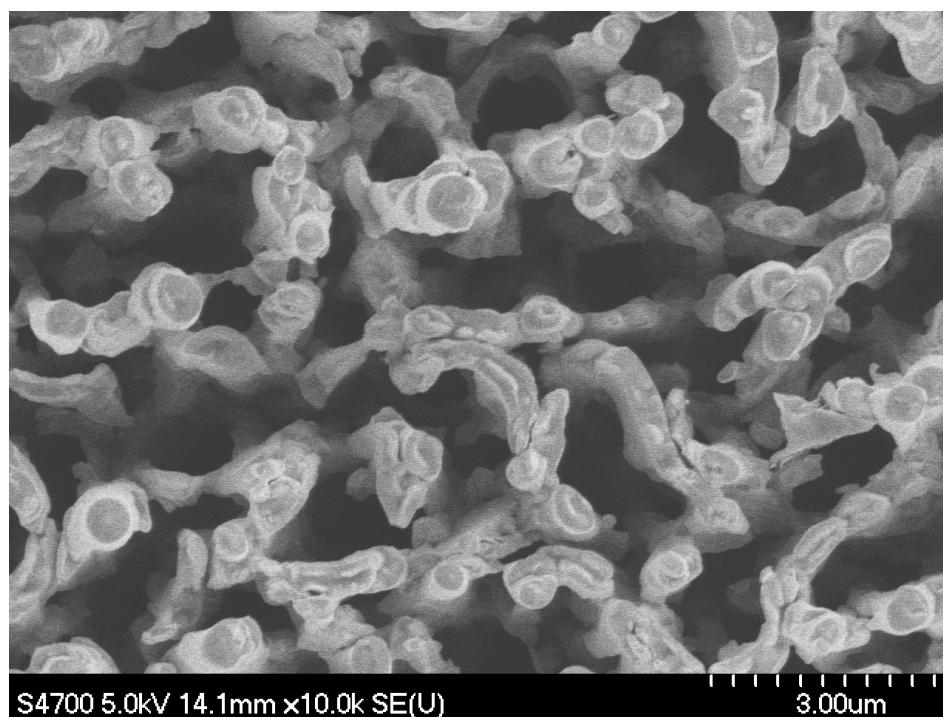
For the purpose of comparison, a meso porous silicon membrane of same dimensions has also been fabricated. The starting material is *p*-type (100) substrates with resistivity of 0.001-0.002 Ω cm. The fabrication processes for the silicon diaphragm is the same as those for macro porous silicon membrane. The anodization process was carried out in a double-tank etching cell with 25% ethanoic HF. Pulsed etching with a peak current density of 75mA/cm² and 1sec/3sec duty cycle was used to produce porous layer with uniform porosity in depth. The total anodization duration lasted for 6 hours. The resulting material has pore sizes of 20nm \sim 40nm. In the heavily doped substrate, the passivated single crystalline silicon layer on the backside is very thin. Therefore, a few hours' backside sputtering etching (6" tool at 100W, 10mTorr) was able to remove that layer and release the meso porous membrane.

6.2 Device Test

For characterizing the PS filter, the setup shown in Figure 6.4 was used. Air was drawn through the PS filter by a vacuum pump. Two 0.8 μ m matched weight membrane filters (MF) were used to sample the upstream and down-stream air of the PS filter respectively. The gas flows through the two MF filters were controlled by needle valves and maintained at the same level. The pressure-drop across the PS filter was monitored by a pressure gauge. By varying the flow rate, the pneumatic characteristic of the PS particle filter could be obtained. As shown in Figure 6.5 (a), the pressure-drop of the macro PS filter is very low (523Pa at 20sccm). Since state-of-art micro scale vacuum pumps are operating at a flow rate less than 1sccm with a pressure capability up to 3000Pa, the macro PS filter will not cause a significant



(a)



(b)

Figure 6.3: SEM images showing (a) the top view and (b) the cross sectional view of the macroporous silicon membrane for particle filtration.

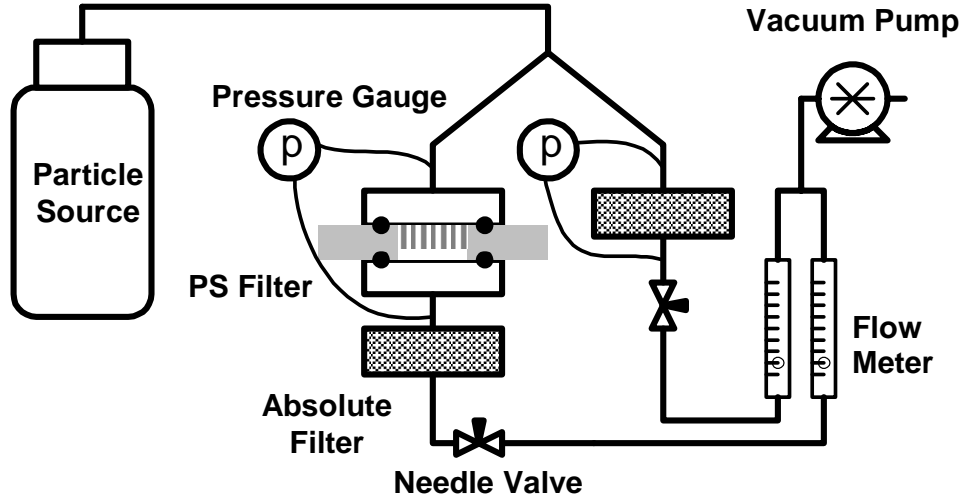


Figure 6.4: Schematic of the experimental setup for testing the macro porous silicon based particle filter.

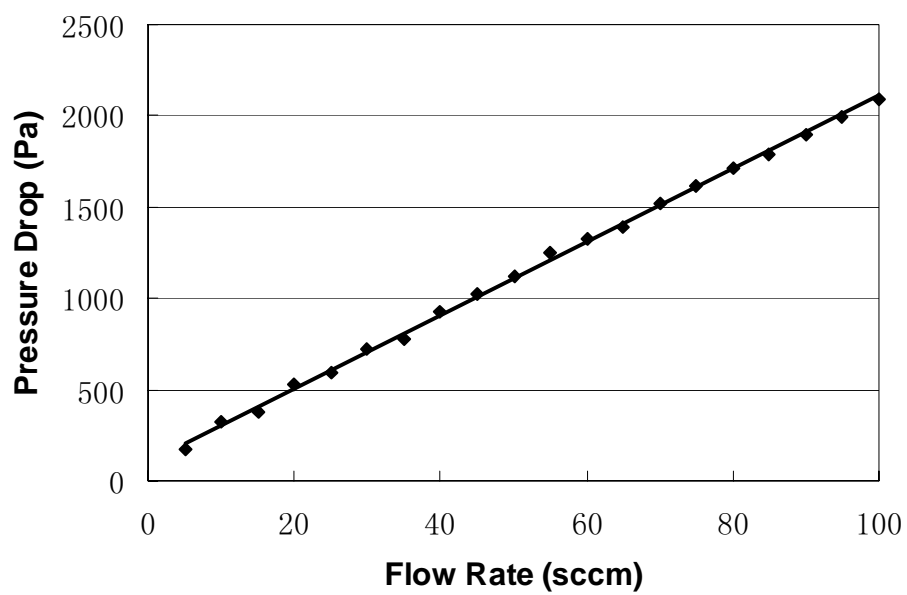
load to a micro scale vacuum pump [90]. This statement, however, is not true for the meso PS filter. Figure 6.5 (b) shows that the meso PS filter's pressure drop is almost twenty times as high as that of the macro PS filter, which makes it inappropriate for the inlet filter application.

For the filtration test, burning incense was used as the particle source. The particle size distribution of the particle source was verified by an Aerodynamic Particle Sizer. As shown in Figure 6.6, most particles have a size in the range of $0.3\text{--}0.8\mu\text{m}$. Since the $0.8\mu\text{m}$ MF filter has a close to zero penetration of particles down to $0.03\mu\text{m}$, it can be considered as an absolute filter in this case [91]. The collection efficiency E of the PS filter in this particle size range can then be determined by gravimetric measurement:

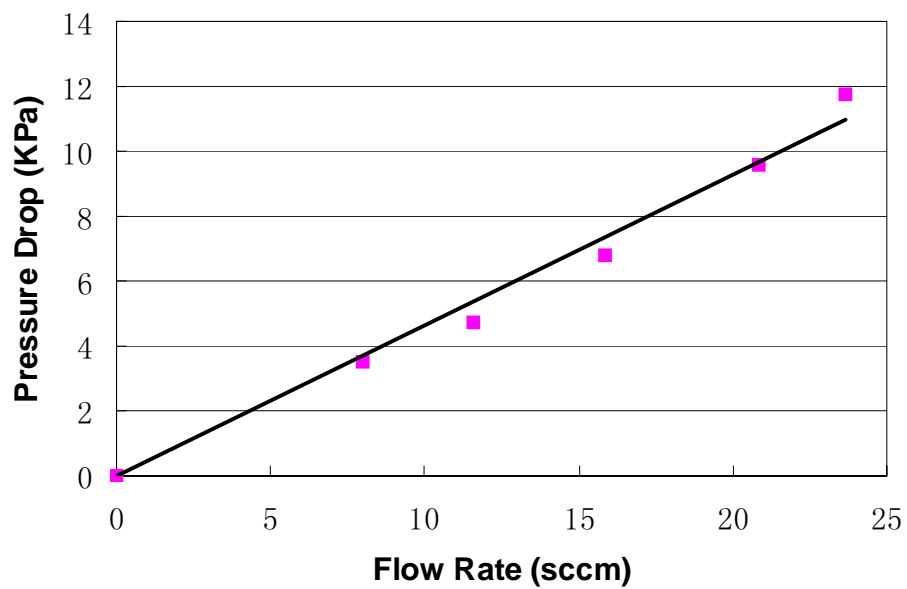
$$E = 1 - \Delta m_d / \Delta m_u \quad (6.1)$$

where Δm_d and Δm_u are the total mass of particles collected by downstream MF filter and upstream MF filter respectively.

The filtration tests were performed at flow rates of 10sccm and 25sccm. In both cases, the pressure-drop across the PS filter showed a two-stage time dependency. In



(a)



(b)

Figure 6.5: Pressure drop of an un-loaded PS particle filter as a function of flow rate for (a) macro porous silicon membrane and (b) meso porous silicon membrane.

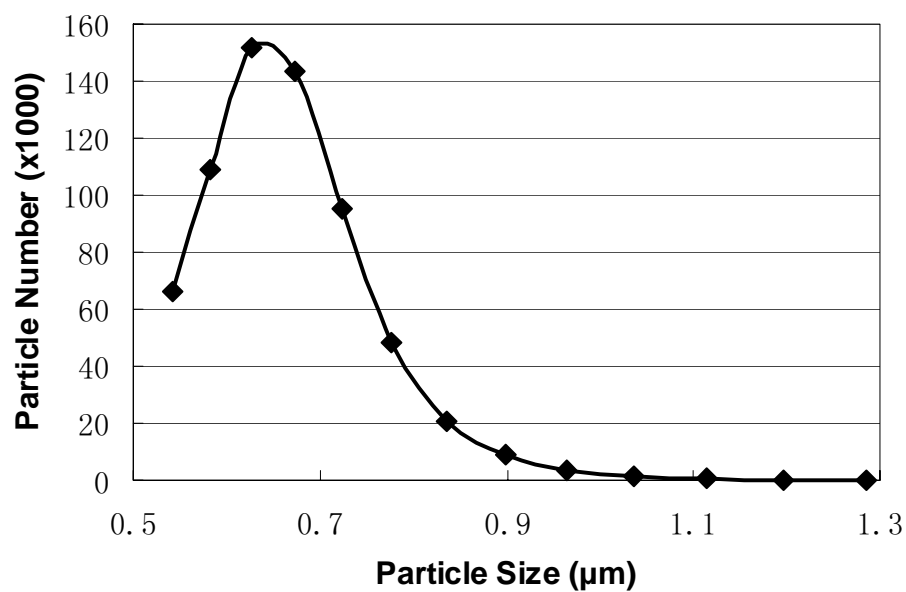


Figure 6.6: Particle size distribution of the particle source used in the filtration test.

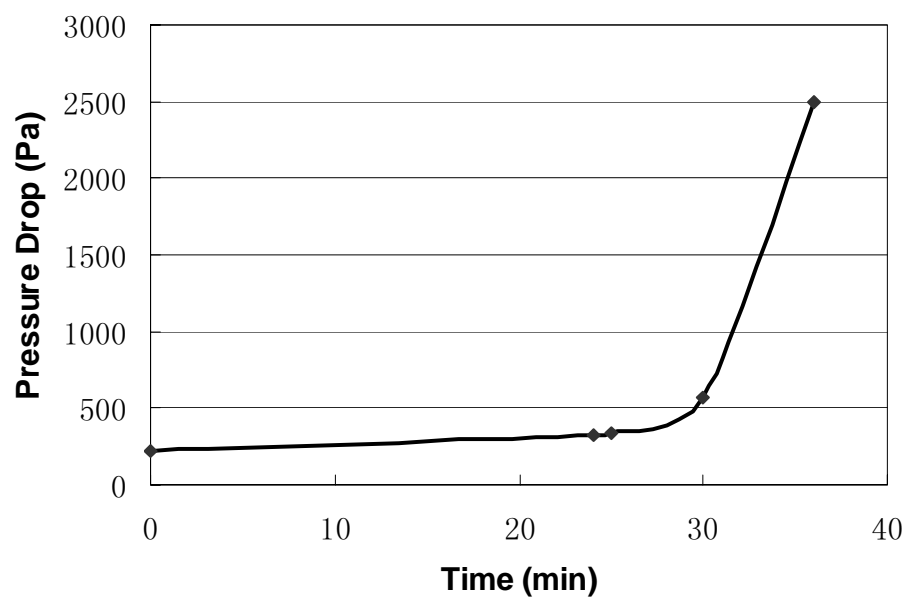


Figure 6.7: The time dependency of the pressure drop across the macroporous silicon membrane with a particle-load flow at 10sccm.

the first phase, a very slow increase in the pressure drop over time was observed, which corresponds to collecting of particles in macro pores and effectively decreasing their diameters. In the second phase, there is a rapid increase in the pressure drop, which corresponds to fully clogged macro pores. Usually, a particle filter should be replaced if it is operating in the second phase. The time dependency of the pressure drop across the PS filter with a particle-loaded flow at 10sccm is shown in Figure 6.7. It should be noted that the lifetime of a particle filter is strongly dependent on how much it has been exposed to particles and can vary in a wide range. Since the particle source used in this filtration test has an extremely high particle concentration, the lifetime of the PS filter was only a half hour, which by no means indicates a low filtration capacity or a short lifetime under normal condition. To avoid ambiguity, a particle filter's capacity is usually measured by the amount of particles collected by the filter during the first filtration phase. For the PS filter, the measured capacity is around $500\mu\text{g}/\text{cm}^2$, which is comparable with those state-of-art particle filters. The filtration efficiency of the PS filter was evaluated as well. After the filtration test, the surface of the upstream MF filter was significantly discoloured and the weight of the upstream MF filter increased by $\sim 180\mu\text{g}$, i.e. $\Delta m_u = 180\mu\text{g}$. The downstream MF filter, on the contrary, had no surface discolouring or measurable mass change, i.e. $\Delta m_d \approx 0$. According to Equation 6.1, these results indicate a nearly 100% collection of particles in the size range of $0.3\mu\text{m}$ to $1\mu\text{m}$ by the PS filter.

The average pore size in the PS filter is $\sim 1.5\mu\text{m}$. However, the filter is able to effectively remove particles in the submicron range. This phenomenon is primarily contributed to the filtration mechanisms of interception and diffusion, as mentioned in Section 2.3. Due to the long ($\sim 120\mu\text{m}$) and tortuous pore paths in the PS filter, both interception and diffusion are pronounced, which enable the filter to capture particles smaller than the openings in the filter. The relatively open structure allows for removing submicron particles while maintaining a low pressure-drop. In addition,

particles were retained along the full depth of the filter. Therefore, the capacity of the depth filter is much higher than those of surface loaded types.

6.3 Mathematical Model of Filtration

In order to understand the contributions of the diffusional component and the interceptional component to the total filter efficiency, a classic mathematical model of filtration has been built for the porous silicon filter. In this filter model, the porous silicon material is approximated as packed fibers of single diameters: single-fiber model [92]. Although this model is very crude compared to the complex morphology of the porous silicon material, it provides an useful insight into the filtration mechanisms and the impacts of different parameters.

Based on the single-fiber model, the overall filter efficiency (E) is given as follows [93]:

$$E = 1 - e^{-E_S S} \quad (6.2)$$

where S is the fiber projected area (dimensionless) and E_S is the single-fiber efficiency. A mathematical definition of the fiber projected area S is:

$$S = \frac{4La}{\pi d_f} \quad (6.3)$$

where L is the length of filter media in the direction of airflow (m), d_f is the fiber diameter (μm), and a is the filter media volume packing density (m^3/m^3). The single-fiber efficiency E_S is the sum of the single-fiber efficiencies by diffusion and interceptions:

$$E_S = E_R + E_D \quad (6.4)$$

where E_R is the interception efficiency and E_D is the diffusion efficiency. Lee and Liu

defined the diffusion efficiency as [94]:

$$E_D = 1.6125 \left(\frac{1-a}{F_K} \right)^{\frac{1}{3}} P_e^{-\frac{2}{3}} \quad (6.5)$$

where F_K is the Kuwabara hydrodynamic factor and P_e is the Peclet number (dimensionless). The Kuwabara hydrodynamic factor is defined as [94–96]:

$$F_K = a - (a^2 + 2\ln a + 3)/4 \quad (6.6)$$

The Peclet number characterizes the intensity of diffusional deposition and is defined as:

$$P_e = \frac{1 \times 10^{-6} U d_f}{D_d} \quad (6.7)$$

where U is the face velocity of the airflow (m/s) and D_d is the particle diffusion coefficient (m²/s) , which can be defined by the Einstein equation:

$$D_d = \mu k T \quad (6.8)$$

where μ is the particle mobility (N·s/m), k is the Boltzman's constant (1.3708×10^{-23} J/K), and T is temperature (K). The particle mobility is defined as:

$$\mu = \frac{C_h}{3 \times 10^{-6} \pi \eta d_p} \quad (6.9)$$

where η is the gas absolute viscosity (1.75×10^{-5} N·s/m²), C_h is Cunningham slip factor (dimensionless), and d_p is particle diameter (μ m). The Cunningham slip factor accounts for the aerodynamic slip that occurs at the particle surface and is defined as:

$$C_h = 1 + \left(\frac{\lambda}{d_p} \right) (2.492 + 0.84e^{-0.435d_p/\lambda}) \quad (6.10)$$

where λ is the gas molecule mean free path (0.067μ m [97]). Liu and Rubow defined

the single-fiber interception efficiency E_R as [96]:

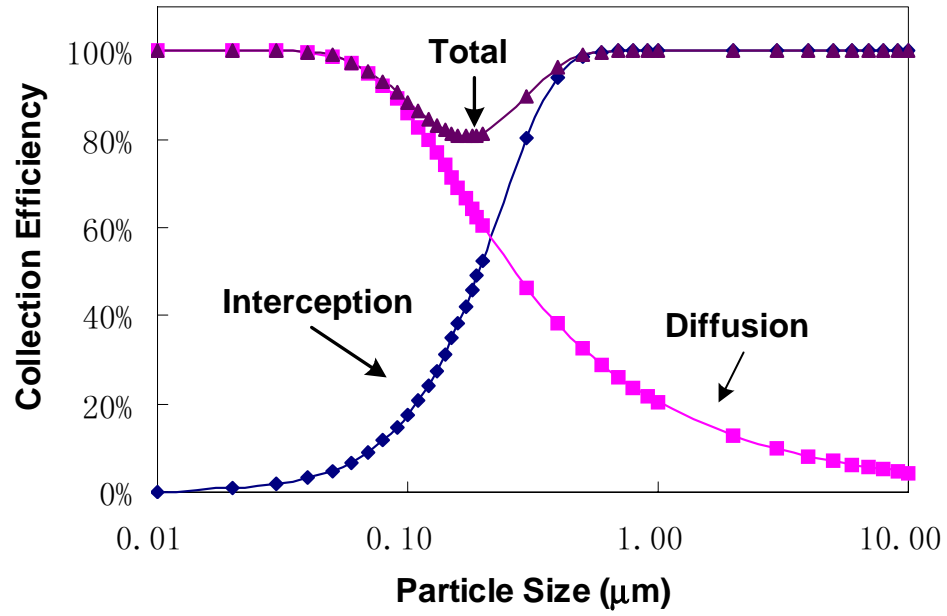
$$E_R = \frac{1}{\epsilon} \left(\frac{1-a}{F_K} \right) \left(\frac{N_r^2}{1+N_r} \right) \quad (6.11)$$

where ϵ is the correction factor that accounts for filter media inhomogeneity and N_r is the interception parameter. The interception parameter is defined as:

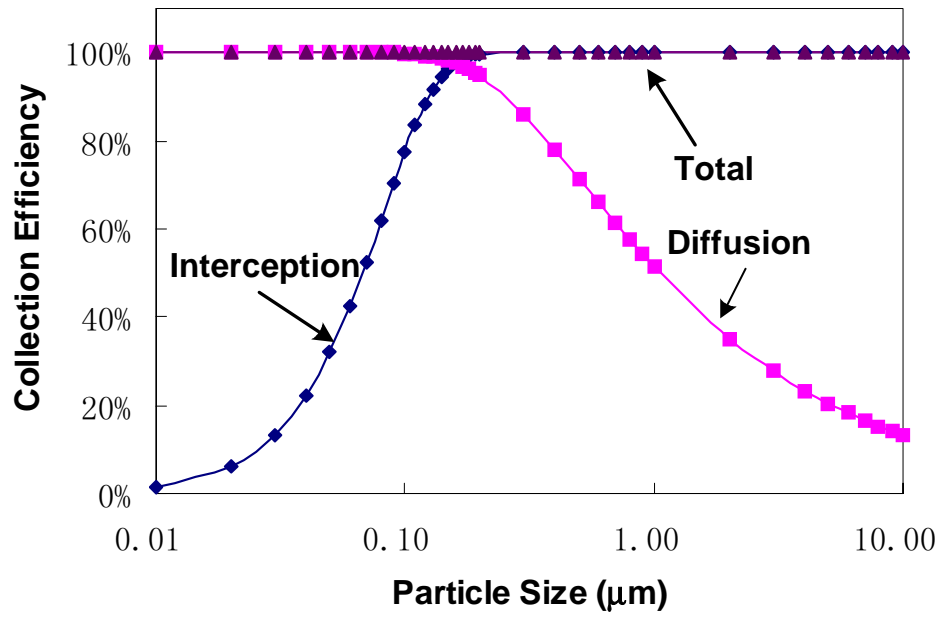
$$N_r = \frac{d_p}{d_f} \quad (6.12)$$

In the single-fiber model defined by Equation 6.2 through Equation 6.12, simulation parameters can be divided into two categories: those that describe the filtration conditions and those that describe the filter structure. The particle size d_p and the face velocity of the airflow U fall into the first category, while the filter's thickness L , the fiber diameter d_f , the fiber packing density a , and the inhomogeneity correction factor ϵ fall into the second category. In the porous silicon material, the fiber diameter d_f is assumed to be equivalent to the average pore diameter. This assumption is the basis of the filtration simulations for membrane filters. The fiber packing density a , on the other hand, can be naturally replaced with $1 - P$, where P is the porosity of the porous material as given by Equation 3.3. It should be noted that in a system of randomly packed fibers, the fiber diameter and the packing density not only impact the size of the opening in the filter but also determine the tortuosity of the fluidic path. Therefore, the above two assumptions are valid only when the porous silicon material has random interconnected pores to imitate a system of randomly packed fibers. For structures of straight pores or relatively straight pores, other types of models, e.g. a capillary model, should be used instead. Since the porous silicon material is fairly homogeneous, ϵ is set to 1 in all simulations.

The simulation results for PS filters with two different pore sizes are shown Figure 6.8. Along with the total filtration efficiency, the diffusion component and the



(a)



(b)

Figure 6.8: Simulation results of the single-fiber models showing the the total filtration efficiency, the diffusion efficiency, and the interception efficiency at face velocity U of 5cm/s (flow rate at 28.86sccm) for porous silicon filters with (a) $L=120\mu\text{m}$, $a=40\%$, and $d_f=3\mu\text{m}$, and (b) $L=120\mu\text{m}$, $a=40\%$, and $d_f=1.5\mu\text{m}$.

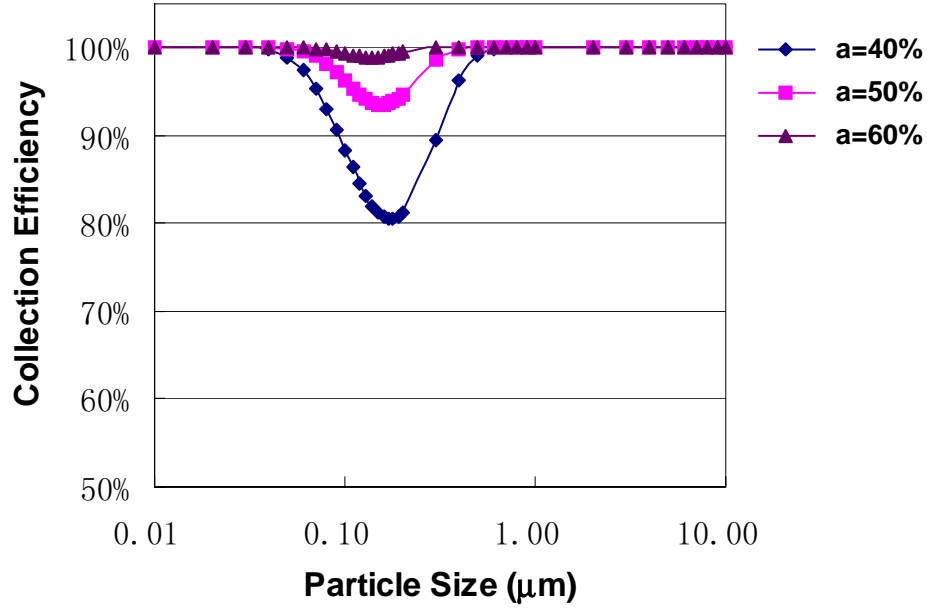


Figure 6.9: Simulated dependency of filtration efficiency on filter's packing density ($d_f=3\mu\text{m}$, $L=120\mu\text{m}$, $U=5\text{cm/s}$). In porous silicon material, a is not an independent parameter, but closely related with pore size.

interception component were plotted as well. They were computed from Equation 6.2 as if each component were a separate filter. Since the diffusion efficiency decreases as the particle size increase while the interception efficiency increases with the particle size, a minimum was observed in the total filtration efficiency where the curves of diffusion efficiency and interception efficiency cross, as shown in Figure 6.8 (a). This minimum efficiency defines the most penetrating particles size. Both the diffusion efficiency and the interception efficiency increase as the pore size decreases. Figure 6.8(a) and (b) show that the minimum filtration efficiency increases from 80.6% to 99.9% as the pore size reduces from $3\mu\text{m}$ to $1.5\mu\text{m}$. This result is consistent with the experimental results presented in the previous section. It shows theoretically that a porous silicon filter with an average pore diameter of $\sim 1.5\mu\text{m}$, a thickness of $120\mu\text{m}$, and a porosity of 60%, i.e. $a=40\%$, is capable of removing submicron particle with a nearly 100% collection efficiency.

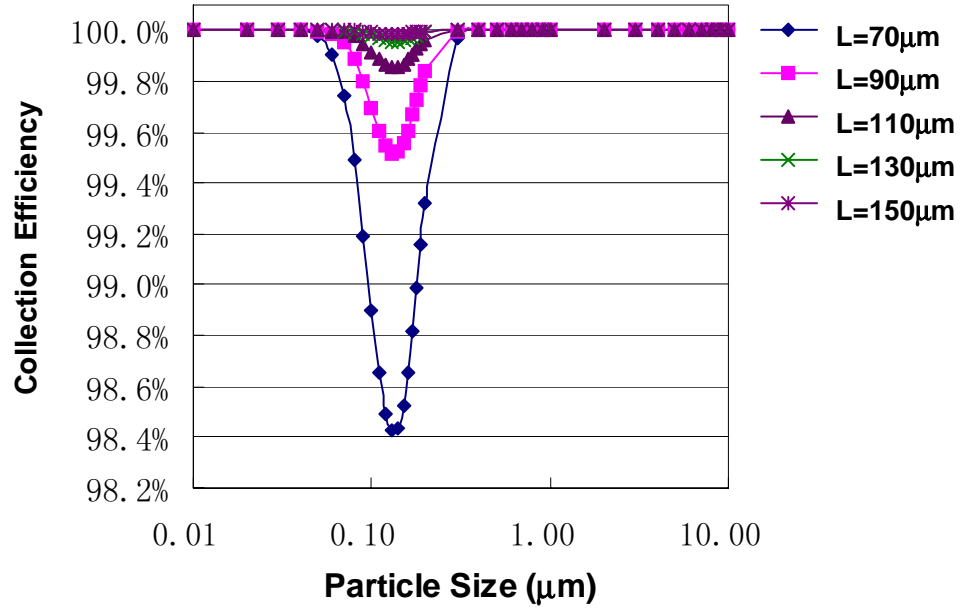


Figure 6.10: Simulated dependency of filtration efficiency on filter's thickness ($a=40\%$, $d_f=1.5\mu\text{m}$, $U=5\text{cm/s}$). The total filtration efficiency increases with filter thickness.

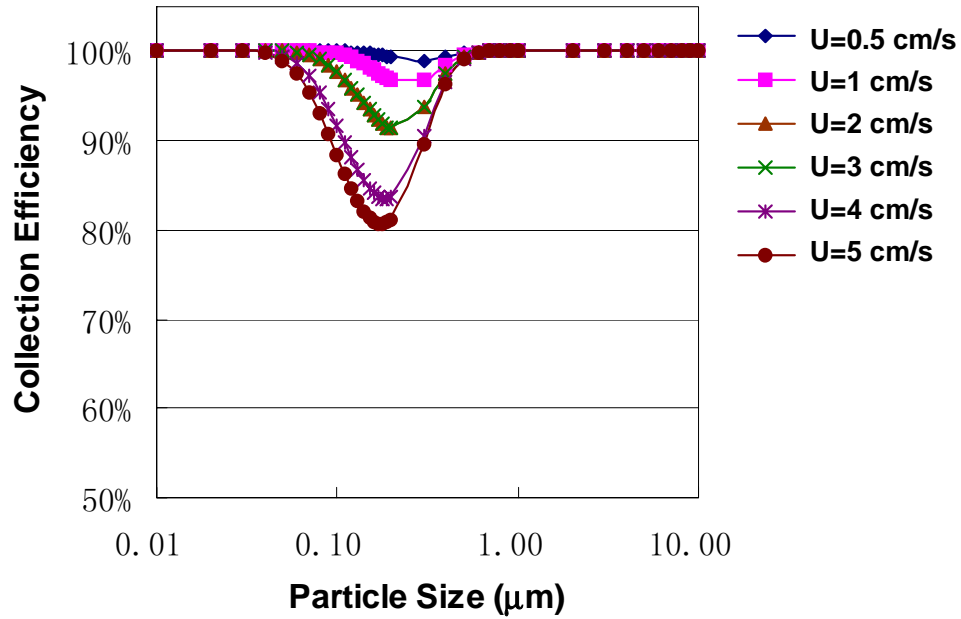


Figure 6.11: Simulated dependency of filtration efficiency on flow's face velocity ($a=40\%$, $d_f=3\mu\text{m}$, $L=120\mu\text{m}$). As the face velocity increases, the total filtration efficiency decreases and the most penetrating particles size decreases as well.

The impact of the packing density on the filtration efficiency is shown in Figure 6.9. The filtration efficiency increases as the packing density increases. It should be remembered that in the porous silicon material a is no longer an independent parameter as in the packed fibrous filters. Instead, a is equal to $1 - P$ and is closely related with pore size. Figure 6.10 shows the dependency of filtration efficiency on the filter's thickness. As expected, the total filtration efficiency increases with filter thickness. Figure 6.11 shows the face velocity's impact on the filtration efficiency. As the face velocity increases, the total filtration efficiency decreases and the most penetrating particles size decreases as well. This is because of the diffusion efficiency's dependency on the particles' residence time in the filter. As face velocity increases, the particles' residence time reduces, which causes the diffusion efficiency curve to shift toward smaller particle size. Therefore, both the most penetrating particle size and the minimum filtration efficiency reduce during this process. Since most micro systems operate at a flow rate of less than 1 sccm, which corresponds to a face velocity of 0.17 cm/s, the impact of face velocity on the filtration efficiency is not a concern for the porous silicon filter.

6.4 Conclusions

Macroporous membranes (3.5 mm diameter \times 120 μ m thickness) with tortuous pores have been fabricated as particle filters for micro systems. The filtration test of the PS filter showed a very large filtration capacity (500 μ g/cm²), a nearly 100% collection efficiency for submicron particles, and a very low pressure-drop. The collection efficiency was further confirmed in a classic mathematical model. The performance of the PS filter is comparable with conventional depth filters, and is suitable for purifying gas samples in a micro system.

Chapter 7

Conclusions

7.1 Contributions

The research presented in this dissertation has led to significant progress in both the development of porous silicon technology and the development of WIMS- μ GC. The major contributions of this work are summarized below.

- The formation process of porous silicon has been extensively studied and characterized as a function of substrate type, doping concentrations, current density profiles, electrolyte compositions. Three different types of porous silicon materials: meso porous silicon, macro porous silicon with straight pores, and macro porous silicon with tortuous pores, have been successfully produced. Anodization conditions have been optimized for producing very thick porous silicon layers, improving pore size uniformity, and obtaining ideal pore morphologies.
- Techniques for masking long anodization processes in hydrofluoric acid have been investigated. Successful masking of etches up to twenty hours have been obtained by an oxide/nitride/polysilicon film stack, prepared by sputter deposition and rapid thermal annealing. By adopting both the Reactive Ion Etching and the BHF wet etching, a method for patterning the masking stack has been developed as well.
- Techniques for forming uniform porous silicon membranes have been investi-

gated. Membranes of full wafer thickness have been achieved at sample scale with a single-step etching process, wherein a sacrificial sample was placed into intimate contact with the backside of the device sample during the anodization to avoid the formation of a passivated single crystalline silicon layer. For a more generic case, a RIE based process has been developed to remove the passivated single crystal Si layer. By utilizing an oxide layer to protect the walls of macro pores, RIE etching was able to remove the passivated silicon layer of non-uniform thickness without damaging the porous silicon structure.

- Si-Au and In-Au bonding techniques have been developed for device assembly. Very low bonding temperature ($\sim 200^{\circ}\text{C}$) and thick/soft bonding layers ($\sim 6\mu\text{m}$) have been achieved by In-Au bonding technology, which is able to compensate for the potentially rough surface on the porous silicon sample without introducing significant thermal stress.
- An integrated calibration vapor source has been designed, fabricated, and tested for the WIMS- μGC . By utilizing a macro porous silicon wick, vapor generation with excellent stability has been achieved. The vapor source has shown uniform and repeatable vapor generation for n-decane with less than a 0.1% variation in 9 hours, and less than a 0.5% variation in rate over 7 days. To our knowledge, this is the first type of calibration vapor source that has been designed for on-board calibration of miniaturized gas/vapor analyzers.
- A porous silicon based particle filter has been fabricated and tested for the WIMS- μGC . By engineering the morphology of the porous silicon membrane, depth filtration with high collection efficiency in the submicron range, low pressure-drop, and large filtration capacity has been achieved. These membranes have demonstrated nearly 100% collection efficiency for particles larger than $0.3\mu\text{m}$ in diameter with a filter capacity of $500\mu\text{g}/\text{cm}^2$. With the PS par-

ticle filter, on-board gas filtration can be achieved for micro analytical systems.

- The feasibility of using porous silicon as the porous media for micro systems has been demonstrated in the integrated calibration source and the inlet filter, thereby introducing new applications of porous silicon technology into the field of micro systems.

7.2 Future Work

For the calibration vapor source, continuing work is needed to obtain stability data over a longer duration of time to fully verify its functionality. In particular, testing of the calibration vapor source in the μ GC system, i.e. interfacing it with the other components including the preconcentrator-focuser (PCF), μ -columns, and μ -sensor array, via the fluidic-interconnection substrate, should be performed. The feasibility of integrating micro valves into the vapor source to further extend its lifetime need to be explored as well. Especially, the impact of the micro valve switching on the stability of the vapor generation rate need to be evaluated.

Porous silicon is a very promising material for gas filtration in micro systems. To take full advantage of its compatibility with micro fabrications process, micromachined prefilters (impactor) should be designed and integrated into the inlet filter to extend its lifetime. In addition, formation of membranes with larger areas need to be explored to provide filters with a larger capacity and lower pressure-drop. If necessary, a honeycomb structure formed by DRIE can be used to support thin membranes of large areas. Modifying the pore surface of the porous silicon material or depositing other functional thin films on the porous silicon structure can also be potential ways to make selective filters or anisotropic membranes.

As mentioned at the beginning of this dissertation, many micro devices can benefit from porous silicon materials. It is hoped that the work presented here will initiate

further research in applying porous silicon materials to the micro systems. As a matter of fact, when this dissertation was being prepared, macro porous silicon membranes were successfully used as the porous media for electro-osmotic pumps. Initial tests in a meso-scale pump body produced a maximum pressure of 5.2KPa and a flow rate of $11.9\mu\text{l}\cdot\text{min}^{-1}\cdot\text{mm}^{-2}$ at 60V, demonstrating macro PS as a promising material for micro scale, high flow-rate/pressure EO pumps. Continuing work is needed to fully characterize the pumping performance, to optimize the porous structure with respect to the pumping efficiency, and to further miniaturize the pump body. The possibility of fully integrating the porous silicon based EO pump should be explored. In particular, issues of priming and bubble generation need to be examined.

Bibliography

- [1] Stephen D. Senturia. *Microsystem Design*. Kluwer Academic Publishers, 2001.
- [2] Richard P. Feynman. There's plenty of room at the bottom. *Journal of Microelectromechanical Systems*, 1(1):60–66, March 1992.
- [3] <http://www.wimserc.org>.
- [4] E. T. Zellers, K. D. Wise, K. Najafi, D. Aslam, R. B. Brown, Q. Y. Cai, J. Driscoll, M. Flynn, J. Giachino, R. Gordenker, M. D. Hsieh, C. T.-C. Nguyen, P. Bergstrom, J. Drelich, C. Friedrich, E. Gamble, M. Kaviany, C. J. Lu, A. Matzger, M. Oborny, S. Pang, J. Potkay, R. Sacks, W.-C. Tian, W. Steinecker, J. Whiting, and Q. Zhong. Determinations of complex vapor mixtures in ambient air with a wireless microanalytical system: Vision, progress, and homeland security applications. In *Digest of IEEE Conference on Technologies for Homeland Security*, pages 92–95, December 2002.
- [5] <http://www.uga.edu/srel/AACES/gchplctutorial.html>.
- [6] <http://www.sandia.gov/mstc/technologies/microanalytical/chemlab.html>.
- [7] Robert L. Grob. Theory of gas chromatography. In Robert L. Grob and Eugene F. Barry, editors, *Modern practice of gas chromatography*. John Wiley & Sons, Inc., 2004.
- [8] E.T. Zellers, W.H. Stinecker, G.R. Lambertus, M. Agah, H.K.L. Chan C.-J. Lu, J.A. Potkay, M.C. Oborny, J.M. Nichols, A. Astle, H.S. Kim, M.P. Rowe, J. Kim, L.W. da Silva, J. Zheng, J.J. Whiting, R.D. Sacks, S.W. Pang, M.Kaviany, P.L. Bergstrom, A.J. Matzger, C. Kurda, L.P. Bernal, K. Najafi, and K.D. Wise. A versatile MEMS gas chromatograph for determinations of environmental vapor mixtures. In *Proceedings of Solid-State sensor, Actuator and Microsystems Workshop*, pages 61–65, Hilton Head Island, June 2004.
- [9] Robert L. Grob and Mary A. Kaiser. Qualitative and quantitative analysis by gas chromatography. In Robert L. Grob and Eugene F. Barry, editors, *Modern practice of gas chromatography*. John Wiley & Sons, Inc., 2004.
- [10] Gary O. Nelson. *Gas mixtures*. Lewis Publishers, 1992.
- [11] Richard D. Sacks. High-speed gas chromatography. In Robert L. Grob and Eugene F. Barry, editors, *Modern practice of gas chromatography*. John Wiley & Sons, Inc., 2004.

- [12] Clyde Orr. *Filtration: Principles and Practices*. MARCEL DEKKER, INC., 1977.
- [13] <http://www.airguard.com/downloads/methodsoffiltration.pdf>.
- [14] Joon Mo Yang, Chih-Ming Ho, Xing Yang, and Yu-Chong Tai. Micromachined particle filter with low power dissipation. *Journal of Fluids Engineering*, 1233:899–908, 2001.
- [15] Göran Stemme and Gjermund Kittilsland. New fluid filter structure in silicon fabricated using a self-aligning technique. *Appl. Phys. Lett.*, 53:1566–1568, 1988.
- [16] Jay K. Tu, Tony Huen, Robert Szema, and Mauro Ferrari. Filtration of sub-100nm particles using a bulk-micromachined direct-bonded silicon filter. *Journal of Biomedical Microdevices*, 1:2:113–119, 1999.
- [17] Hironobu Sato, Takayuki Kakinuma, Jeung Sang Go, and Shuichi Shoji. A novel fabrication of in-channel 3-d micromesh structure using maskless multi-angle exposure and its microfilter application. In *Proceedings of IEEE The Sixteenth Annual International Conference on Micro Electro Mechanical Systems*, pages 223–226, Kyoto, January 2003.
- [18] Yong-Kyu Yoon, Jung-Hwan Park, Florent Cros, and Mark G. Allen. Integrated vertical screen microfilter system using inclined su-8 structures. In *Proceedings of IEEE The Sixteenth Annual International Conference on Micro Electro Mechanical Systems*, pages 227–230, Kyoto, January 2003.
- [19] <http://www.millipore.com>.
- [20] A Uhler. Electrolytic shaping of germanium and silicon. *The Bell System Technical Journal*, 35:333–347, 1956.
- [21] Y. Wanatabe, Y. Arita, T. Yokoyama, and Y. Igarashi. Formation and properties of porous silicon and its applications. *J. Electrochem. Soc.: Solid-State Science and Technology*, 122(10):1352–1355, 1975.
- [22] K. Imai. A new dielectric isolation method using porous silicon. *Solid-State Electronics*, 24:159–164, 1981.
- [23] L.T. Canham. Silicon quantum wire array fabricated by electrochemical and chemical dissolution of wafers. *Appl. Phys. Lett.*, 57(10):159–164, 1990.
- [24] Leigh Canham, editor. *Properties of Porous Silicon*. INSPEC, 1997.
- [25] A. Halimaoui, C. Oules, G. Bomchil, A. Bsiesy, F. Gaspard, R. Herino, M. Ligeon, and F. Müller. Electroluminescence in the visible range during anodic-oxidation of porous silicon films. *Appl. Phys. Lett.*, 59(3):304–306, 1991.

- [26] Z.M. Rittersma, A. Splinter, A. Bödecker, and W. Benecke. A novel surface-micromachined capacitive porous silicon humidity sensor. *Sensors and Actuators B*, 68:210–217, 2000.
- [27] G.M. O’Halloran, M. Kuhal, P.J. Trimp, and P.J. French. The effect of additives on the adsorption properties of porous silicon. *Sensors and Actuators A*, 61:415–420, 1997.
- [28] G.M. O’Halloran, P.M. Sarro, J. Groeneweg, P.J. Trimp, and P.J. French. A bulk micromachined humidity sensor based on porous silicon. In *Transducers ’97*, pages 563–566, June 1997.
- [29] Hee-Kyung Min, Ho-Sik Yang, and Sung M. Cho. Extremely sensitive optical sensing of ethanol using porous silicon. *Sensors and Actuators B*, 67:199–202, 2000.
- [30] C. Baratto, E. Comini, G. Faglia, G. Sberveglieri, G. Di Francia, F. De Filippo, V. La Ferrara, L. Quercia, and L. Lancellotti. Gas detection with a porous silicon based sensor. *Sensors and Actuators B*, 65:257–259, 2000.
- [31] W.M. Kwok, Y.C. Bow, W.Y. Chan, M.C. Poon, P.G. Han, and H. Wong. Study of porous silicon gas sensor. In *Proceedings of Electron Devices Meeting*, pages 80–83, June 1999.
- [32] Alexandra Splinter, Olaf Bartels, and Wolfgang Benecke. Thick porous silicon formation using implanted mask technology. *Sensors and Actuators B*, 76:354–360, 2001.
- [33] T. Taliencia, M. Dilhan, E. Massone, A. Foucaran, A.M. Gué, T. Bretagnon, B. Fraisse, and L. Montès. Porous silicon membranes for gas-sensor applications. *Sensors and Actuators A*, 46-47:43–46, 1995.
- [34] C. Tsamis, A.G. Nassiopoulou, and A. Tserepi. Thermal properties of suspended porous silicon micro-hotplates for sensor applications. *Sensors and Actuators B*, 95:78–82, 2003.
- [35] S.S. Tsao. Porous silicon techniques for SOI structures. *IEEE Circuits and Devices magazines*, pages 1–7, November 1987.
- [36] G. Kaltsas and A.G. Nassiopoulou. Frontside bulk silicon micromachining using porous-silicon technology. *Sensors and Actuators A*, 65:175–179, 1998.
- [37] W. Lang, P. Steiner, U. Schaber, and A. Richter. A thin film bolometer using porous silicon technology. *Sensors and Actuators A*, 43:185–187, 1994.
- [38] T.E. Bell, P.T.J. Gennissen, D. DeMunter, and M. Kuhl. Porous silicon as a sacrificial material. *J. Micromech. Microeng*, 6:361–369, 1996.

- [39] V. Lehmann and H. Föll. Formation mechanism and properties of electrochemically etched trenches in n -type silicon. *J. Electrochem. Soc.*, 137(2):653–659, February 1990.
- [40] F. Müller, A. Birner, J. Schilling, U. Gösele, Ch. Kettner, and P. Hänggi. Membranes for micropumps from macroporous silicon. *phys. stat. sol.(a)*, 182:585–590, 2000.
- [41] F. Müller, A. Birner, U. Gösele, V. Lehmann, S. Ottow, and H. Föll. Structuring of macroporous silicon for applications as photonic crystals. *J. Electrochem. Soc.*, 137(2):653–659, 1990.
- [42] V. Lehmann and U. Grüning. The limits of macropore array fabrication. *Thin Solid Films*, 297:13–17, 1997.
- [43] K.J. Chao, S.C. Kao, C.M. Yang, M.S. Hseu, and T.G. Tsai. Formation of high aspect ratio macropore array on p -type silicon. *Electrochemical and Solid-State Letters*, 3(10):489–492, 2000.
- [44] H. Föll, M. Christophersen, J. Carstensen, and G. Hasse. Formation and application of porous silicon. *Materials Science and Engineering R*, 39:93–141, 2002.
- [45] M. Christophersen, J. Carstensen, A. Feuerhake, and H. Föll. Crystal orientation and electrolyte dependence for macropore nucleation and stable growth on p -type Si. *Materials Science and Engineering B*, 69-70:194–198, 2000.
- [46] V. Lehmann, W. Hönlein, H. reisinger, A. Spitzer, H. Wendt, and J. Willer. A novel capacitor technology based on porous silicon. *Thin Solid Films*, 297:138–142, 1996.
- [47] F. Müller, A. Birner, U. Gösele, V. Lehmann, S. Ottow, and H. Föll. Applications of microstructured porous silicon as a biocatalytic surface. *phys. stat. sol.(a)*, 182:495–504, 2000.
- [48] U. Grüning, V. Lehmann, S. Ottow, and K. Busch. Macroporous silicon with a complete two-dimensional photonic band gap centered at $5\mu\text{m}$. *Appl. Phys. Lett.*, 68:747–749, 1996.
- [49] V. Lehmann. Trends in fabrication and applications of macroporous silicon. *phys. stat. sol.(a)*, 197(1):13–15, 2003.
- [50] S. Ottow, V. Lehmann, and H. Föll. Processing of three-dimensional microstructures using macroporous n -type silicon. *J. Electrochem. Soc.*, 143(1):385–390, 1996.
- [51] V. Lehmann and S. Rönnebeck. MEMS techniques applied to the fabrication of anti-scatter grids for x-ray imaging. In *Proceedings of The 14th IEEE International Conference on Micro Electro Mechanical Systems*, pages 84–85, January 2001.

- [52] A. Halimaoui. Porous silicon: material processing, properties and applications. In J.C. Vial and J. Derrien, editors, *Porous silicon science and technology*. Springer-Verlag, 1995.
- [53] D. Pagonis, G. Kaltsas, and A.G. Nassiopoulou. Implantation masking technology for selective porous silicon formation. *phys. stat. sol.(a)*, 197(1):241–245, 2003.
- [54] Jun-Hwan Sim, Sung-Ho Hahm, Jung-Hee Lee, Jong-Hyun Lee, In-Sik Yu, and Jin-Sup Kim. Eight-beam piezoresistive accelerometer fabricated by using a selective porous silicon etching method. In *Transducers '97*, pages 1193–1196, June 1997.
- [55] St. Frohnhoff, M.G. Berger, M. Thönissen, C. Dieker, L. Vescan, H. Münder, and H. Luth. Formation techniques for porous silicon superlattices. *Thin Solid Films*, 255:59–62, 1995.
- [56] V. Lehmann and U. Gösele. Porous silicon formation: a quantum wire effect. *Appl. Phys. Lett.*, 58(8):856–858, 1991.
- [57] G. Vincent. Optical properties of porous silicon superlattices. *Appl. Phys. Lett.*, 64(18):2367–2369, 1994.
- [58] Tracy Bell. *A cochlear implant fabricated using a bulk silicon surface micromachining process*. PhD thesis, The University of Michigan, 1999.
- [59] R. Willem Tjerkstra, Johannes G. E. Gardeniers, John J. Kelly, and Albert van den Berg. Multi-walled microchannels: free-standing porous silicon membranes for use in μ TAS. *Journal of Microelectromechanical Systems*, 9(4):495–501, December 2000.
- [60] Gerhard Lemmel, Sandra Schweizer, Sébastien Schiesser, and Philippe Renaud. Tunable optical filter of porous silicon as key component for a MEMS spectrometer. *Journal of Microelectromechanical Systems*, 11(6):815–827, December 2002.
- [61] Takao Yonehara and Kiyofumi Sakaguchi. Eltran[®]: novel SOI wafer technology. *JSAP International*, 4:10–16, July 2001.
- [62] John J. Kelly, Xinghua H. Xia, Colin M. A. Ashruf, and Paddy J. French. Galvanic cell formation: a review of approaches to silicon etching for sensor fabrication. *IEEE Sensors Journal*, 1:127–142, August 2001.
- [63] R.L. Smith and S.D. Collins. Porous silicon formation mechanisms. *J. Appl. Phys.*, 71(8):R1–R22, April 1992.
- [64] V. Lehmann. The physics of macroporous silicon formation. *Thin Solid Films*, 255:1–4, 1995.
- [65] U. Gösele and V. Lehmann. Porous silicon quantum sponge structures: formation mechanism, preparation methods and some properties. In Zhe Chuang Feng and Raphael TSU, editors, *Porous silicon*. World Scientific, 1994.

- [66] O. Teschke, M.C. Dos Santos, M.U. Kleinke, D.M. Soares, and D.S. Galvao. Spatially variable reaction in the formation of anodically grown porous silicon structures. *J. Appl. Phys.*, 78(1):590–592, July 1995.
- [67] Y.H. Seo, K.S. Nahm, M.H. An, E-K. Suh, Y.H. Lee, and H.J. Lee. Formation mechanism and pore size control of light-emitting porous silicon. *Jpn. J. Appl. Phys.*, 33:6425–6430, 1994.
- [68] J. Carstensen, M. Christophersen, and H. Föll. Pore formation mechanisms for the Si–HF system. *Materials Science and Engineering*, B69-70:23–28, 2000.
- [69] M. Christophersen, J. Carstensen, and H. Föll. Crystal orientation dependence of macropore formation of n-type silicon. *Phys. Stat. Sol (a)*, 182(2):601–606, 2000.
- [70] M. Christophersen, J. Carstensen, and H. Föll. Crystal orientation dependence of macropore formation in p-type silicon using organic electrolytes. *Phys. Stat. Sol (a)*, 182(1):103–107, 2000.
- [71] F. Gaspard, A. Bsiesy, M. Ligeon, F. Muller, and R. Herino. Charge exchange mechanism responsible for *p*-type silicon dissolution during porous silicon formation. *J. Electrochem. Soc.*, 136(10):3043–3046, October 1989.
- [72] V. Lehmann, R. Stengl, and A. Luigart. On the morphology and the electrochemical formation mechanism of mesoporous silicon. *Materials Science and Engineering*, B69-70:11–22, 2000.
- [73] V. Lehmann. The physics of macropore formation in low doped *n*-type silicon. *J. Electrochem. Soc.*, 140(10):2836–2843, October 1993.
- [74] <http://www.tf.uni-kiel.de/matwis/amat/index.html>.
- [75] L.T. Canham, A.G. Cullis, C. Pickering, O.D. Dosser, T.I. Cox, and T.P. Lynch. Luminescent anodized silicon aerocrystal networks prepared by supercritical drying. *Nature*, 368:133–135, 1994.
- [76] Ulrike Grüning and Arthur Yelon. Capillary and van der waals forces and mechanical stability of porous silicon. *Thin Solid Films*, 255:135–138, 1994.
- [77] G. Amato, V. Bullara, N. Brunetto, and L. Boarino. Drying of porous silicon: a raman, electron microscopy, and photoluminescence study. *Nature*, 276:204–207, 1996.
- [78] M. Hejjo Al Rifai, M. Christophersen, S. Ottow, J. Carstensen, and H. Föll. Dependence of macropore formation in n-Si on potential, temperature, and doping. *Journal of The Electrochemical Society*, 147:627–635, 2000.
- [79] http://www.tf.uni-kiel.de/matwis/amat/semi.en/kap_3/illustr/i3_1_2.html.

- [80] M. Christophersen, S. Langa, J. Carstensen, I. M. Tiginyanu, and H. Föll. A comparison of pores in silicon and pores in iii-v compound materials. *Physica Status Solidi A*, 197:197–203, 2003.
- [81] M. L. Schattenburg, C. Chen, P. N. Everett, J. Ferrera, P. Konkola, and Henry I. Smith. Sub-100 nm metrology using interferometrically produced fiducials. *J. Vac. Sci. Technol. B*, 17(6):2692–2697, 1999.
- [82] J.H. Song and M.J. Sailor. Dimethyl sulfoxide as a mild oxidizing agent for porous silicon and its effect on photoluminescence. *Inorg. Chem.*, 37:3355–3360, 1998.
- [83] Volker Lehmann. Barcoded molecules. *Nature Materials*, 11:12–13, 2002.
- [84] H. Ohji, P. J. Trimp, and P. J. French. Fabrication of free standing structure using single step electrochemical etching in hydrofluoric acid. *Sensors and Actuators A*, 73:95–100, 1999.
- [85] R.F. Wolffenbuttel and K.D. Wise. Low-temperature silicon wafer-to-wafer bonding using gold at eutectic temperature. *Sensors and Actuators A*, 43:223–229, 1994.
- [86] R.F. Wolffenbuttel. Low-temperature intermediate Au-Si wafer bonding; eutectic or silicide bond. *Sensors and Actuators A*, 62:680–686, 1997.
- [87] Chin C. Lee, Chen Y. Wang, and Goran Matijasevic. Au-in bonding below the eutectic temperature. *IEEE Trans. on Components, Hybrids, and Manufacturing Technology*, 16:311–316, 1993.
- [88] M. C. Oborny, J. Zheng, J. M. Nichols, C-J. Lu, P. L. Bergstrom, R. P. Manginell, G. C. Frye-Mason, and E. T. Zellers. Passive calibration-vapor source for a micro gas chromatograph. In *Proceedings of 7th International Conference on Miniaturized Chemical and Biochemical Analysts Systems*, pages 1243–1246, Squaw Valley, October 2003.
- [89] Craig. R. Friedrich and P. J. Coane. Micromilling development and applications for microfabrication. *Journal of Microelectronic Engineering*, 35:367–372, 1997.
- [90] A. Astle, L. Bernal, P. Washabaugh, H. Kim, and K. Najafi. Theoretical and experimental performance of a high frequency micropump. In *Proceedings of 2005 ASME International Mechanical Engineering Congress*, Orlando FL, 2003.
- [91] N. Montassier, L. Dupin, and D. Boulaud. Experimental study on the collection efficiency of membrane filters. *J. Aerosol Sci.*, 27:S637–S638, 1996.
- [92] W. J. Kowalski, William Bahnfleth, and T. S. Whittam. Filtration of airborne microorganisms: Modeling and prediction. *ASHRAE Transactions: Research*, 105(2):4–17, 1999.

- [93] C.N. Davies. *Air filtration*. Academic Press, 1973.
- [94] M.J. Matteson and Clyde Orr, editors. *Filtration: Principles and Practices*. MARCEL DEKKER, INC., 1987.
- [95] R.C. Brown. *Air filtration*. Pergamon Press, 1993.
- [96] B.Y.H. Liu and K.L. Rubow. Fluid filtration : gas. In *Air filtration by fibrous media*. American Society for Testing and Materials, 1986.
- [97] P.C. Reist. *Aerosol science and technology*. McGraw-Hill, 1993.