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## Fabrication and characterization of room temperature operating single electron transistors using focused ion beam technologies

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FABRICATION AND CHARACTERIZATION OF ROOM TEMPERATURE  
OPERATING SINGLE ELECTRON TRANSISTORS USING FOCUSED ION  
BEAM TECHNOLOGIES

By

PRASANJIT SANTOSH KUMAR KARRE

A DISSERTATION

Submitted in partial fulfillment of the requirements

for the degree of

DOCTOR OF PHILOSOPHY

(Electrical Engineering)

MICHIGAN TECHNOLOGICAL UNIVERSITY

2008

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This dissertation, "**Fabrication and Characterization of Room Temperature operating Single Electron Transistors Using Focused Ion Beam Technologies**", is hereby approved in partial fulfillment of the requirements for the degree of DOCTOR OF PHILOSOPHY in the field of Electrical Engineering.

DEPARTMENT:  
Electrical and Computer Engineering

Signatures:

Dissertation Advisor \_\_\_\_\_

Dr. Paul L. Bergstrom

Committee \_\_\_\_\_

Dr. Anand Kulkarni

\_\_\_\_\_  
Dr. Warren Perger

\_\_\_\_\_  
Dr. Yoke Khin Yap

\_\_\_\_\_  
Dr. Shashi P. Karna

Department Chair \_\_\_\_\_

Dr. Leonard J. Bohmann

Date \_\_\_\_\_

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Houghton, Michigan

P. Santosh Kumar Karre

January,2008

## Dedication

To

my parents

Smt & Sri: Bharathi and Kumar Karre

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## Abstract

The single electron transistor (SET) is a Coulomb blockade device, whose operation is based on the controlled manipulation of individual electrons. Single electron transistors show immense potential to be used in future ultra lowpower devices, high density memory and also in high precision electrometry. Most SET devices operate at cryogenic temperatures, because the charging energy is much smaller than the thermal oscillations. The room temperature operation of these devices is possible with sub-10nm nano-islands due to the inverse dependance of charging energy on the radius of the conducting nano-island. The fabrication of sub-10nm features with existing lithographic techniques is a technological challenge. Here we present the results for the first room temperature operating SET device fabricated using Focused Ion Beam deposition technology. The SET device, incorporates an array of tungsten nano-islands with an average diameter of 8nm. The SET devices shows clear Coulomb blockade for different gate voltages at room temperature. The charging energy of the device was calculated to be 160.0 meV; the capacitance per junction was found to be 0.94 atto F; and the tunnel resistance per junction was calculated to be 1.26 G  $\Omega$ . The tunnel resistance is five orders of magnitude larger than the quantum of resistance (26 k  $\Omega$ ) and allows for the localization of electrons on the tungsten nano-island. The lower capacitance of the device combined with the high tunnel resistance, allows for the Coulomb blockade effects observed at room temperature. Different device configurations, minimizing the total capacitance of the device have been explored. The effect of

the geometry of the nano electrodes on the device characteristics has been presented. Simulated device characteristics, based on the soliton model have been discussed. The first application of SET device as a gas sensor has been demonstrated.

# Chapter 1

## Introduction

### 1.1 Introduction

The tremendous growth observed in the microelectronics industry for the past four decades is made possible by the demand to have high computing power and large data storage. These requirements have increased the momentum of research and development efforts both in the semiconductor industry and academia. The progress was made possible by miniaturizing the device dimensions, resulting in better performance and higher component packing density [1]. The basic field effect transistor (FET) invented forty years ago is a remarkable device and is a basic building block of all the modern electronics. The continuous scaling of the complementary metal-oxide semiconductor (CMOS), resulted in advances like, the increase in device density,

reduction in power dissipation, improvements in the circuit speed and reduction in the cost per chip [2]. The semiconductor industry has entered nanotechnology regime with the introduction of 0.13  $\mu m$  technology node having 70nm gate length with sub-2.0nm gate oxide thickness. Different silicon technologies have been introduced to continue scaling and improve the CMOS device performance. With the reduction in device dimensions, scaling is confronted with fundamental limitations based on the material, and the physical dimensions of the device. Intense research is being carried both in industry and academia on new electronic materials and non silicon devices and their integration on to the existing CMOS technology. The emerging nano technologies are finding potential applications in many branches of science and engineering, like health, environment, energy conversion and storage and sensing [3]

## 1.2 CMOS Scaling

The generalized scaling approach followed in reducing the device dimensions of the transistor over four decades is based on the scaling theory [4]. It was recognized during early 1970s, by Mead [5] and Dennard [6] that the MOS transistor can be scaled based on few technology parameters, including the basic transistor geometry. It was this realization of scaling theory and its practical application, that made possible the better known “Moore’s Law”. The phenomenological observation, that the



transistors are becoming smaller by a factor of two, becoming faster and cheaper for every 18 months is known as Moore's Law [7]. The scaling of the transistors not only increased the device density but also improved the device performance [8]. Different scaling methods include, the constant field scaling and constant voltage scaling. The scaling method mostly used is the constant field scaling. In constant field scaling the field strengths (and profiles) in the MOS transistor remain the same across the different process generations, thus making it a constant field scaling. The constant electric field scaling has vital effect on the power density. The reduction in the feature size following the constant field scaling considered the leakage currents to be not significant, but with the scaling of the devices reaching 90nm node with 50-70nm gate lengths, with the supply voltages 1-1.2V, leakage power forms a significant part of the total power, because of the subthreshold nonscaling the threshold voltage cannot be scaled without a limit. With the continued scaling, the system performance is degrading because of the subthreshold leakages. The reduction in the supply voltage to maintain constant field results in the decrease on the drain current. The drive currents are increased by using thinner gate oxides and lower threshold voltage, strained silicon is also used as a process enhancement for increasing the on current of the transistor without increasing the off current [9]. At the 65nm technology node, the thickness of the gate oxide is 1.2nm which is few monolayers of Si-O bonds [10], increasing the difficulty to scale the gate oxide further. Reduction in the gate leakage is obtained by using high k-gate dielectrics while maintaining a very low electrical equivalent oxide

thickness. Hot carrier injection effects become prominent at lower device dimensions because of the scattering and /or impact ionization. Hot carrier injection effects can be reduced by placing lightly doped drain (LDD) implants. The RC time delays are expected to increase because of scaling and RC time delays can be reduced by using low k- dielectrics. The introduction of low k dielectrics is much slower than predicted by the ITRS roadmap due to both mechanical and electrical weaknesses [11; 12]. With scaling, the impact of Joule heating in metals will become even more pronounced because of the lower thermal conductivity of the low-k dielectric films.

### 1.3 Emerging Technologies

The main impediments to the CMOS scaling are the subthreshold leakage and the gate-dielectric leakage. Double/multi-gate MOSFETs [13] or FinFET [14] in which a second gate is added opposite to the traditional gate, have been recognized for their potential to better control the short-channel effects. Silicon on insulator (SOI) has shown suppression of short channel effects and drain induced barrier lowering. Vertical MOSFET configuration provides other new device options for higher levels of functional integration. Advanced engineering solutions coupled with some of the non classical CMOS technologies like the single gate and multi gate CMOS technologies have been demonstrated to improve the device performance. This would continue

the CMOS scaling until some time into the future, till the gate lengths of transistors approach 10nm. No potential solutions are foreseen for device structures below 10nm. For sub-10nm gate lengths, the CMOS is going to face some of the fundamental limitations. The materials will not obey the bulk properties at these nano scales and the devices will behave differently because of the inherent quantum effects which will dominate at these device dimensions [15]. Nano-devices based on the quantum effects are a possible solution for the next generation electronic devices. Some of the possible candidates are the 1-D structures (Carbon nanotubes and nano-wires), spintronic devices, resonant tunneling devices, single electronics, molecular electronic devices, Ferro magnetic logic devices, devices based on quantum cellular automata. The emerging nano-devices would not replace the existing CMOS devices, but would complement the CMOS devices [16]. When the MOSFETs reach the ultimate limits of scaling, single electron effects will be inevitable at the sub 10nm device dimensions and hence some perceive the Single Electron Devices to be a natural successor to the MOSFETs. Hence Single Electron devices are of immense interest. Single Electron Devices operate on a simple principle of Coulomb Blockade, and can manipulate electrons at the level of elementary charge, hence their operation is guaranteed even if the dimensions of the device are reduced to a molecular level. The Single Electron Devices not only function as simple switching device but also show immense potential for large scale integration. Single electron transistors (SETs) are the most fundamental three terminal Single electron devices. SET devices are show immense potential

in high-density device integration for memory applications, ultra low power devices [17; 18; 19; 20; 21] and nano sensing. Despite the observation of single electron effects a quarter century ago [22], the progress towards, the room temperature operating SETs is rather slow [23]. There is a need for technologies enabling the fabrication of room temperature operating single electron transistors.

## 1.4 Motivations and Goals

As a technology development project the main goal of this project is the realization of room temperature operating Single Electron Transistors, using Focused Ion beam technologies. The specific objectives of the project include:

- † Characterization of the Focused Ion Beam system.
- † Characterization of FIB etch and deposition process.
- † Materials development for the realization of SETs.
- † Development of process flow for the realization of room temperature operating Single Electron Transistors.
- † Design and modeling of the SET devices.
- † Demonstration of coulomb blockade in SET at room temperature.

† Demonstration of coulomb oscillations at room temperature.

† SET device characterization.

## 1.5 Dissertation Outline

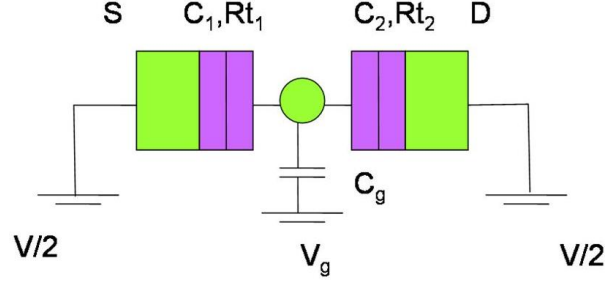
The dissertation starts with the introduction chapter, where the effects of MOSFET scaling on the device behavior is presented along with the emerging solutions to the scaling of the MOSFETS. Chapter 2 describes the single electron transistor behavior using a soliton model, and explains the device design. The description of Focused Ion Beam technologies, the method for the fabrication of conducting nano-islands in tungsten using FIB deposition and the application of FIB technologies towards the fabrication of SET device at MTU is presented in Chapter 3. Results for the fabricated SET device characteristics are presented in Chapter 4. The analysis of the device characteristics and comparison to the simulated device characteristics, the application of the SET device towards gas sensing are presented in Chapter 5. Chapter 6 summarizes the research findings and suggests directions for future work.

# Chapter 2

## Single Electron Transistors and Device Design

### 2.1 The Single Electron Transistor

Single electronics has the potential to be used as a future building block of nano-scaled electronic devices [24; 25]. The basic element of SET is the tunnel junction with very small capacitance, the current conduction in SET is controlled by the quantum mechanical tunneling of the electrons through the tunnel barrier. The device structure of the SET is composed of two ultra small tunnel junctions in series separated by a conducting nano-island and a gate electrode which can be resistively or capacitively coupled to the central conducting island as shown in Figure 2.1. The tunnel junction



**Figure 2.1:** Schematic of Single Electron Transistor.

is characterized by a tunnel resistance  $Rt_1$  and a capacitance of  $C_1$ , similarly the other tunnel junction with tunnel resistance  $Rt_2$  and a capacitance of  $C_2$ , and  $C_g$  is the gate capacitance . When the gate terminal of SET is resistively coupled it is known as R-SET, when capacitively coupled it is known as C-SET. In the present work only capacitively coupled SETs are considered.

The orthodox theory describes the single electron device characteristics based on the electrostatics of the system [26]. The assumptions made by the orthodox theory are

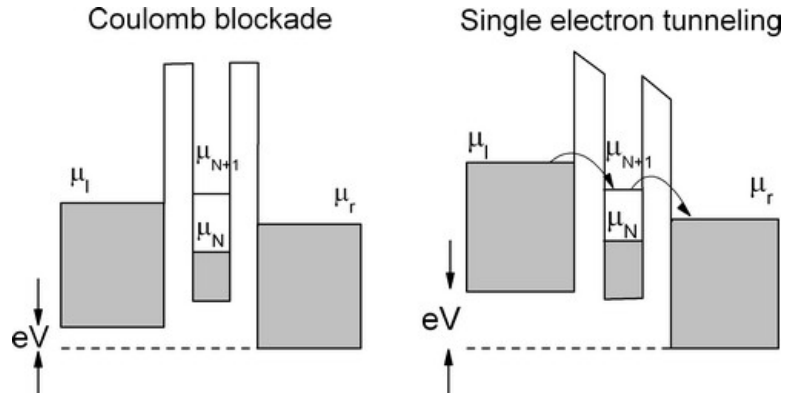
- † The quantization of electron energy levels inside the conducting nano-island is ignored.
- † The electron tunneling time scale  $t_\tau$  through the potential barrier is negligibly small compared to other time scales.
- † Several simultaneous tunneling events (Co-tunneling) are ignored.

Despite these assumptions the orthodox theory is in agreement with the experimental

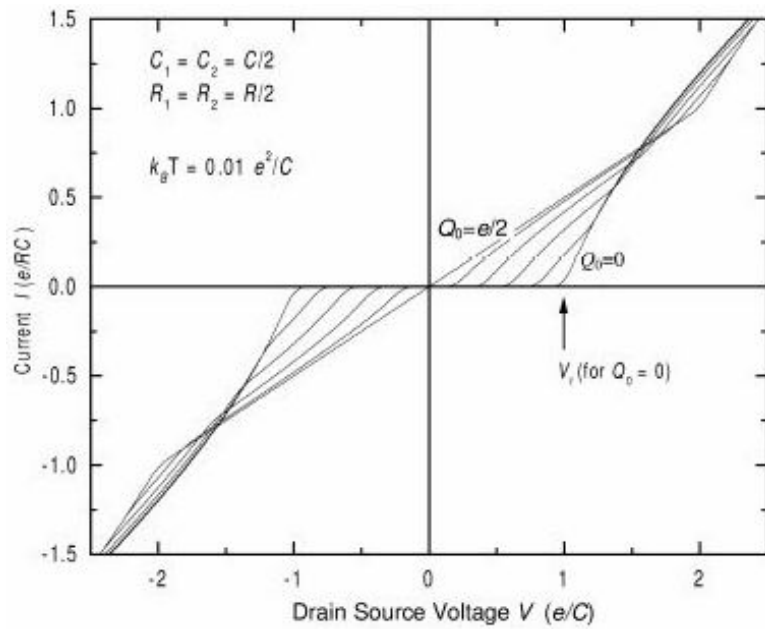
data obtained for the single dot SET systems. The tunneling of electrons through the barrier depends on the electrostatics of the system. The Figure 2.2 shows the Coulomb blockade and single electron tunneling, where  $\mu_l$  and  $\mu_r$  represent the chemical potential of the left and right electrode respectively,  $\mu_N$  and  $\mu_{N+1}$  are the chemical potentials for the highest and first available electron state of the system [27]. The confinement of electrons on to the central confining island in SET results in discrete energy levels in the conducting island. The energy required to add an electron to the conducting island is the charging energy  $E_C = e^2/C$ . In SET system the minimum energy needed for electron tunneling from Source to the conducting island is the charging energy. The external applied bias provides the energy for tunneling. The Coulomb blockade is a situation when there is no electron tunneling, because, the applied bias cannot provide energy greater than the charging energy, resulting in the OFF state of the device. The non-linear  $I$ - $V$  characteristics of the device shown in Figure 2.3 show the Coulomb blockade effect for low voltages less than  $e/C$  the dc current is suppressed.

The ambient thermal noise also provides energy for tunneling. Coulomb blockade events are smeared out if the charging energy  $E_C$  is less than the thermal energy  $\kappa_B T$ . Hence charging energy should be higher than the thermal energy. After a threshold voltage  $V_t = e^2/C$  the coulomb blockade is overcome and the current approaches one of its linear asymptotes. For a SET the threshold voltage, as well as the source-drain current, are a periodic function of the gate voltage. The periodicity is given by  $e/C_g$ .



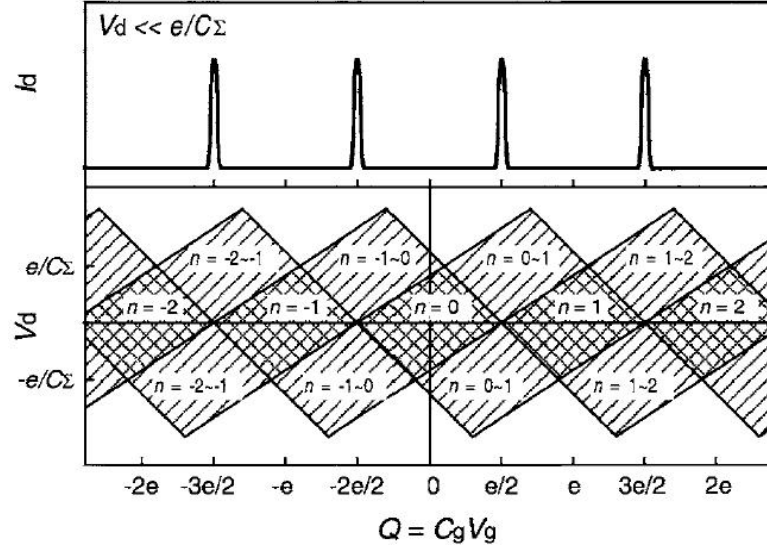


**Figure 2.2:** Coulomb blockade and single electron tunneling of a single dot SET



**Figure 2.3:**  $I_D$ - $V_{DS}$  Characteristics of a single dot SET

Reproduced by permission of the publisher from K.K. Likharev, Single-Electron Devices and Their Applications, Proceedings of the IEEE, Vol. 87, No. 4, pp. 606-632, April 1999. Fig. 6. (b), ©1999 IEEE.



**Figure 2.4:**  $I_D$ - $V_{GS}$  Characteristics of a single dot SET .

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The application of gate voltage shifts the discrete energy levels on the confining island, the shifting energy levels allow for the electrons to tunnel on to the confining island. The discrete nature of the energy levels creates a periodic increase in the source-drain current with the variation of gate voltage. The Figure 2.4 shows the periodic increase in drain current with the gate voltage. The regions, where the current is not increasing are electrostatically stable, and are called Coulomb diamonds. When the electrostatics of the SET system becomes unstable with the increase in gate voltage, the system becomes stable with the transfer of an electron.

The requirements for the room temperature operating SET devices are that the tunnel resistance  $R_t$  of the device should be higher than the quantum of resistance  $R_K$ ,

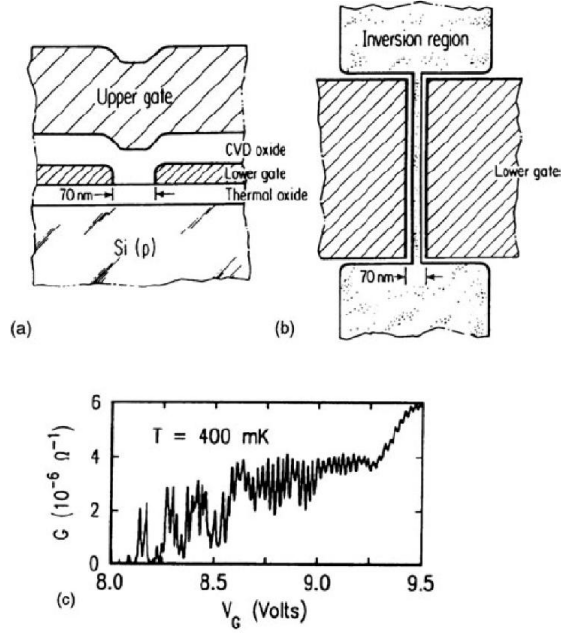
which is  $R_K = \frac{h}{e^2}$ , this condition ensures the confinement of electrons to the central island, resulting in the discreteness of energy levels. Fabrication techniques enabling sub-10 nm feature size are indispensable for fabricating SET devices, operable at room temperature. Various SET structures [21; 28] have been experimentally fabricated. Most of the SET devices operate at low temperatures. To observe the charging effects at room temperature, the charging energy  $E_C = e^2/C$  should be greater than the thermal energy  $\kappa_B T$ . For a temperature of 300K, the capacitance of the device should be in the order of atto Farads  $aF$  for room temperature operation. The capacitance of the device is made up of the capacitance of the tunnel junctions, the capacitance of the quantum island, and the capacitance of the gate terminal. From the initial studies on Single Electron systems, mainly metals and III-V compound semiconductors have been used to investigate the basic physics of the transport and to explore possible applications, because of the ease of confinement of electrons possible in the two dimensional electron gas (2DEG) in III-V compounds. The material requirements for the SET are that, the central island can be made of semiconducting material or a metal. The metallic central island is studied in the present work.

### 2.1.1 Semiconductor based Single Electron Transistor

The first reported work on Si SETs was performed in 1989 by Scott-Thomas et al [29; 30]. The observed CB oscillation in conductance was attributed to Si islands unintentionally formed in a narrow one-dimensional channel in a double-gate Si MOS-

FET, as shown in Figure 2.5. The confinement of electrons was created by forming a narrow one dimensional channel in silicon by forming an inversion layer. Lateral confinement is obtained using the X-ray lithography. The islands formed by this method resulted in charging energies  $E_c$  of less than 1.0 meV. The island size was further reduced by using a silicon on insulator (SOI) layer of separation by implanted oxygen (SIMOX) process. The first SOI wafer used in SET fabrication was reported by Ali and Ahmed [31]. The  $E_c$  reported by this method was 1.6 meV, the island size was still limited by lithography, and the coulomb blockade (CB) effects observed at few Kelvin temperatures. The first room temperature operating Coulomb Blockade oscillations using silicon was reported by Takahashi et al [32] using the pattern dependent-oxidation (PADOX) process where a wide silicon nano-wire connected at both the ends is oxidized to form a short silicon nano wire. After the thermal oxidation, tunnel junctions were formed in the silicon nano-wire, the tunnel junctions were formed because of the bandgap modulation of Si due to quantum confinement and oxidation induced stress. The device showed the charging energies in the range of 10-50 meV [33].

Improved version of PADOX called vertical-PADOX (V-PADOX) uses thermal oxidation of a long silicon wire with a thickness modulation, resulting in higher charging energies shown in Figure 2.6. It is recognized that silicon wire based SETs could provide higher temperature operation but, one of the main issues with the PADOX and V-PADOX methods of fabrication of SETs is the reproducibility concerning the



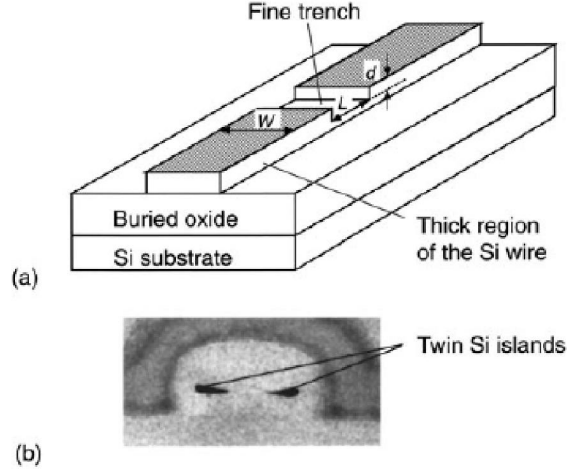
**Figure 2.5:** Silicon SET with dual gate MOS structure .

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tunnel barrier fabrication [34; 35]. The tunnel barrier formation can be controlled by the side wall depletion gates as suggested by Kim et al., as shown in Figure 2.7

Instead of relying on lithography to reduce the size of silicon, non lithographical techniques, based on the nucleation of silicon to produce the silicon nano-crystals, was investigated as shown in Figure 2.8. Tunnel currents through a single Si nano-crystal was measured using AFM. Dutta et al. [36; 37] reported SETs with silicon nano-crystals, where the charging energies were in the range of few tens of meV.

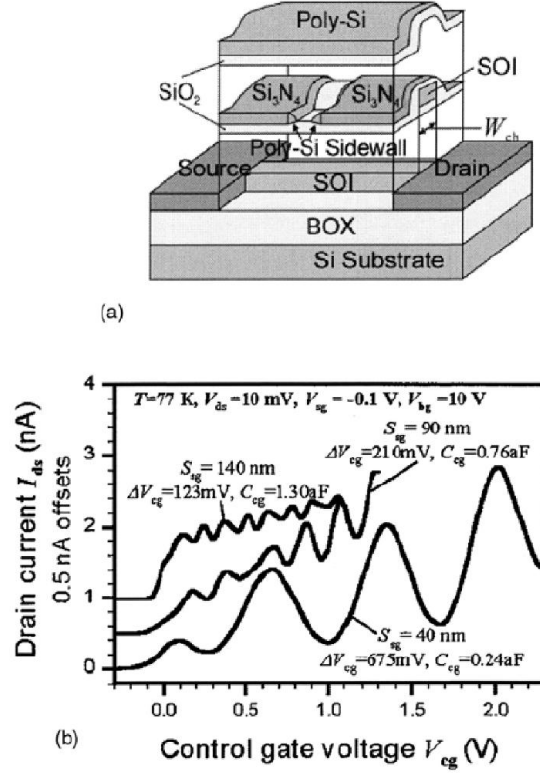
The nano-crystals of 8nm were deposited using VHF-Plasma CVD technique, on



**Figure 2.6:** SET Fabrication by V-PADOX method .

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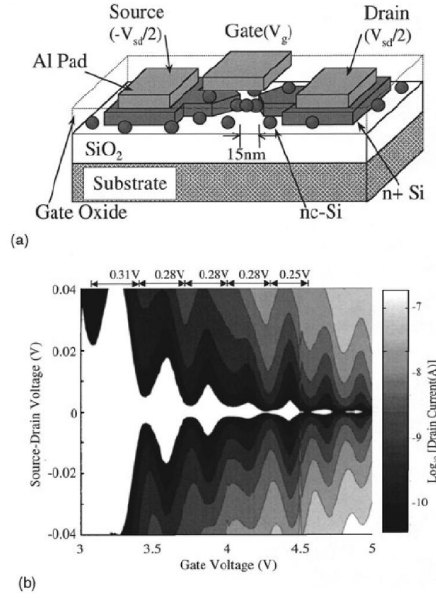
which the source drain electrodes were formed. SETs with  $E_C$  of few meV were observed. Uchida et al [25] used thin SOI to fabricate SETs with  $E_C$  of 35.0 meV. The most important issue with the Si based SETs, is the random fabrication of tunnel junctions, and the precise placement of the electrodes at the desired location. The lack of controllability of the positioning of the Si nano-crystals in the desired place is resulting in devices with non repeatable device parameters. Single Electron Transistors are realized in other semiconductor materials than silicon, by achieving the two dimensional confinement of electrons using hetro-structures. The total confinement of electrons is achieved by fabricating the electrodes on the surface of the two-dimensional electron gas (2DEG) hetero-structures, such as GaAs. The applied bias to the electrodes under suitable conditions creates a small region of (2DEG)



**Figure 2.7:** Sidewall depleted gates on SOI [33]

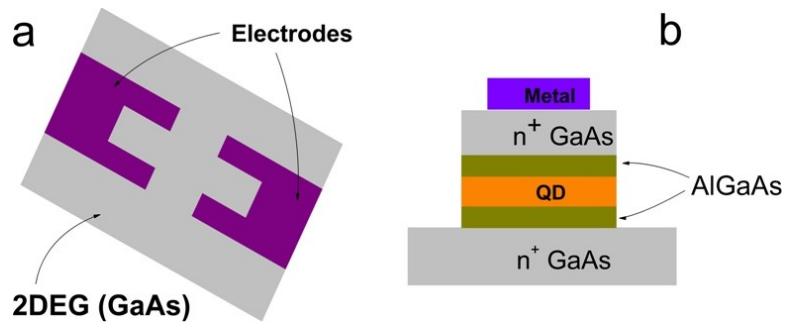
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which is isolated from the remainder of (2DEG) called as planar quantum dots. Thus is the basis of creating the confined electron gas at the center. In contrast SETs can also be realized using a different scheme, where, the flow of current is vertical with respect to the hetero-structure layer, such structures are called as vertical quantum dots. In such nano-structures the electrons are confined by both the vertical confinement provided by AlGaAs or other large gap materials and the in-plane confinement is provided by lithography [38]. The pictorial view of the planar and vertical quantum



**Figure 2.8:** Si nano crystal based SET.

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**Figure 2.9:** a: Planar quantum dot and b: Vertical quantum dot .

dots can be seen in the Figure 2.9.



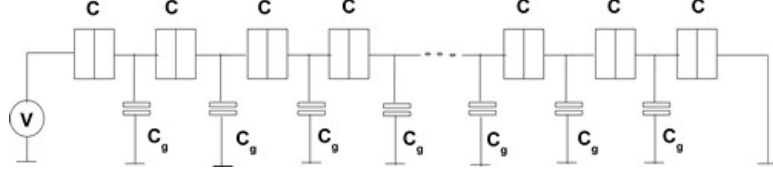
### 2.1.2 Non Semiconductor based Single Electron Transistor

The first experimental demonstration of SETs was reported with metal/oxide system in 1987 by T.A. Fulton and G.J Dalon [22]. These devices, however, did not exhibit the Coulomb diamond characteristic at room temperature because of the large island size and large capacitance of the SET. One of the requirements to observe single charge tunneling in nano-scale junction systems, is that the metallic islands should be connected to the other metallic regions only via tunnel barriers with tunneling resistance. Fabrication of SETs using angle evaporation technique was reported by Pashkin et al [39], the Al SET was fabricated using e-beam lithography show the room temperature operation. The feature size of the fabricated structure was reduced by using dry oxidation, Takahashi et al [40], reported a room-temperature Si-based SET based on this technique. Nb/Nb oxide SETs with extremely high charging energy were fabricated using the scanning probe microscope (SPM)based anodization technique and thermal oxidation as reported by Shirakashi et al [41]. SETs with Ti/-TiOx systems were fabricated using atomic-force-microscope(AFM) based oxidation technique by Matsumoto et al. [42]. Semiconducting carbon nanotube was used as the SET island, by doping potassium in to single wall carbon nano tube to form the island, the device exhibited SET behaviour at 160k, this work was reported in 2000 by Jing Kong et al [43]. However, such approaches have limited ability to reproducibly create controlled size nanoislands at desired locations on a technologically useful substrate. The present work looks at the possible technologies for the fabrication of room

temperature operating SETs, which can be fabricated, more reliably and much faster than some of the existing techniques, using focused ion beam technologies.

## 2.2 Model for the device characteristics of a multi dot SET system

The non-linear device characteristics of the single dot SET device can be explained using the orthodox theory [44], which considers the two tunnel junction system. In a multi dot SET system, there are  $N$  number of tunnel junctions depending on the number of conducting islands participating in the conduction process. There are few models which extend the orthodox theory to three junction system to explain the device characteristics. The device characteristics of a multi dot SET system can be explained using the charge soliton analysis [45] in which, the multi dot SET system can be analyzed as an array of tunnel junctions. For an array of  $N$  tunnel junctions, the capacitance of each junction is assumed to be equal to  $C$ , the capacitance of the gate is denoted by  $C_g$ . The capacitive coupling between the neighbors and next neighbors is neglected. The injection of electron in to an array of conducting islands modulate the charge in the system, as the electron tunnels from one conducting island to the next, the charge on the conducting island is varied and the neighboring conducting islands are polarized by the presence of the extra charge on the conducting island. A schematic diagram of an array of tunnel junctions is shown in the Figure 2.10.



**Figure 2.10:** Schematic diagram of an array of tunnel junctions.

The tunnel junctions are assumed to symmetric, meaning all the tunnel junctions are assumed to have the same value of tunnel junction capacitance and resistance. The self capacitance of the islands are also assumed to be equal, thus making the array of tunnel junctions homogeneous. The array is biased with a differential voltage of  $V$  volts. The injection of an electron in to the array creates a potential distribution. The potential distribution takes on the form of a charge soliton, and as one soliton enters the array, the probability for the next soliton entering the array is reduced. The repelling force between the soliton and the biased edge drives the propagation of the charge soliton in to the array and to the other end of the array, thus creating the Coulomb Blockade effect. The potential of an arbitrary island defined by  $i$  as a function of the distance from the charged conducting island  $k$  is calculated to be Equation (2.1) [46].

$$V_i = \frac{e}{C_{eff}} [\exp((-|i - k|) \operatorname{arccosh}(1 + \frac{C_g}{2C}))] \quad (2.1)$$

Where  $C_{eff} = \sqrt{C_g^2 + 4CC_g}$ . The potential does not change its form and hence called a soliton. The potential falls off exponentially with a characteristic fall off length.

The charging energy of the system is dependent on the effective capacitance of the array as  $E_C = \frac{e^2}{2C_{eff}}$ .  $E_l$ , and  $E_r$  are the energies applied to the tunnel junctions on left and right respectively because of the applied voltage. The  $I$ - $V$  characteristics of the two junction system can be solved by knowing the electron transition probability from the state  $N$  to the adjacent state  $N+1$  or  $N-1$ . If  $r_1$  Equation (2.2) and  $l_1$  as shown in Equation (2.3) are the tunneling rates from the right and the left of the junctions as a function of the number of electrons and the applied voltage, the source drain characteristics can be obtained from the calculations of the tunneling rates [47; 48; 49; 50; 51].

$$r_1(N, V) = \frac{1}{e^2 R} \left\{ \frac{E_r - E_c}{1 - \exp\left[\frac{E_r - E_c}{k_B T}\right]} \right\} \quad (2.2)$$

$$l_1(N, V) = \frac{1}{e^2 R} \left\{ \frac{E_l - E_c}{1 - \exp\left[\frac{E_l - E_c}{k_B T}\right]} \right\} \quad (2.3)$$

The average current can be calculated using the tunneling rates, as Equation (2.4)

$$I = \sum e[r_1(N, V) - l_1(N, V)]\rho(N, V) \quad (2.4)$$

Where  $\rho(N, V)$  is the probability that there are  $N$  extra electrons on the island.

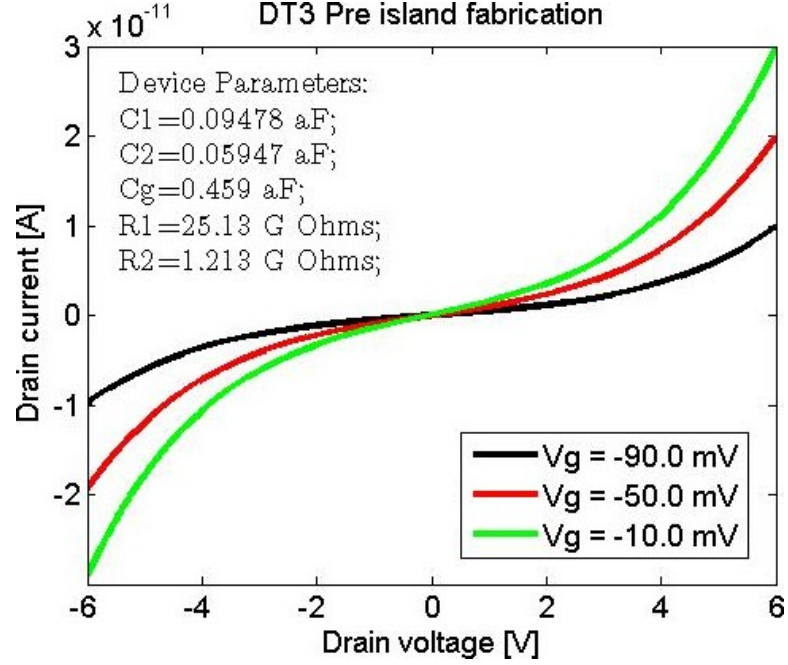
For an array of  $n$  tunnel junctions, the master equation method of solving for the

$I$ - $V$  characteristics, can be used by replacing the potentials by the charge soliton potentials and calculating the tunneling rates, for the array of tunnel junctions. The basic model used for a single dot SET system [52], has been used in the simulation of the non linear device characteristics, with the incorporation of soliton charge potential for a multi dot SET system. The simulated  $I$ - $V$  characteristics for an array of ten islands are obtained using the above explained method, the simulated device characteristics are shown in the Figure 2.11. The parameters of the array which are used for the simulation of the Coulomb Blockade characteristics are summarized in the Table 2.1.

**Table 2.1:** Device parameters used for the simulation of  $I$ - $V$  characteristics of a multidot SET system having ten conducting islands

Device Parameter	Value
$C_1$	$0.0947 \times 10^{-18} \text{ F}$
$C_2$	$0.05947 \times 10^{-18} \text{ F}$
$C_g$	$0.459 \times 10^{-18} \text{ F}$
$R_1$	$25.13 \times 10^9 \Omega$
$R_2$	$1.213 \times 10^9 \Omega$

It is seen from the simulated  $I$ - $V$  characteristics in Figure 2.11 that a clear Coulomb Blockade effect is observable. As the gate voltage decreases the slope of the characteristics is increasing thereby increasing the average amount of current obtained because of tunneling. The gate capacitance of SET system is assumed to be ten times higher than the tunnel junction capacitance, which is  $0.0947 \text{ aF}$ . The tunnel resistance of the left tunnel junction ( $R_1$ ) is assumed to be ten times higher than the tunnel resistance



**Figure 2.11:** Simulated Nonlinear  $I$ - $V$  Characteristics of multi dot SET

of the right tunnel junction ( $R_2$ ). The device parameters used in the simulation of the non linear device characteristics are obtained from the experimental results. The device parameters are extracted, assuming the tunnel junctions are homogenous, the device parameter extraction is explained in section 5.2. From the simulated source-drain characteristics of the multi dot SET system, it can be concluded that the device behavior can be predicted using the soilton model.

## 2.3 Single Electron Transistor Design

The Single Electron Transistors, in the present work are fabricated using Focused Ion Beam (FIB) processing. Both FIB etching and FIB deposition methods have been investigated for the fabrication of SET devices [53; 54; 55; 56]. The present section describes the design of SET devices, based on the features size that can be fabricated using FIB etching and deposition capabilities of the Hitachi FB-2000A FIB instrument.

The important requirements for the room temperature operation of SETs are the following:

- † Small capacitance of the device.
- † Large tunnel resistance of the tunnel junctions.
- † Higher charging energy  $E_C$  than the thermal energy  $\kappa_B T$ .

The capacitance of the device is made up of the capacitance of the tunnel junctions, the capacitance of the central conducting island, the capacitance between the gate and the conducting island. The capacitance of the island is the dominant factor, and hence by reducing the capacitance of the island the overall capacitance of the device can be minimized. The estimated capacitance of the device for room temperature operation is few atto Farads  $aF$ . The tunnel resistance of the tunnel junctions, on

both sides of the conducting island, are very important in confining the electronic wave function on to the central conducting island, higher the tunnel resistance, the better is the confinement of electrons. The minimum tunnel resistance required for the confinement of electrons on to the central conducting islands is equal to the quantum of resistance, which is  $\hbar/e^2$ , numerically equal to 25.6 k  $\Omega$ . The charging energy of the device,  $E_C = e^2/2C$ , is dependent on the capacitance of the device. The charging of the device is higher when the overall capacitance of the device is small. The charging energy of the device should be more than thermal energy at room temperature, for the observation of Coulomb blockade effects at room temperature. The design of the device should include all the above factors in order to achieve the room temperature operation of the SET device. The following section will discuss the design of SET, using FIB etching and FIB deposition.

### 2.3.1 SET based on FIB Etching

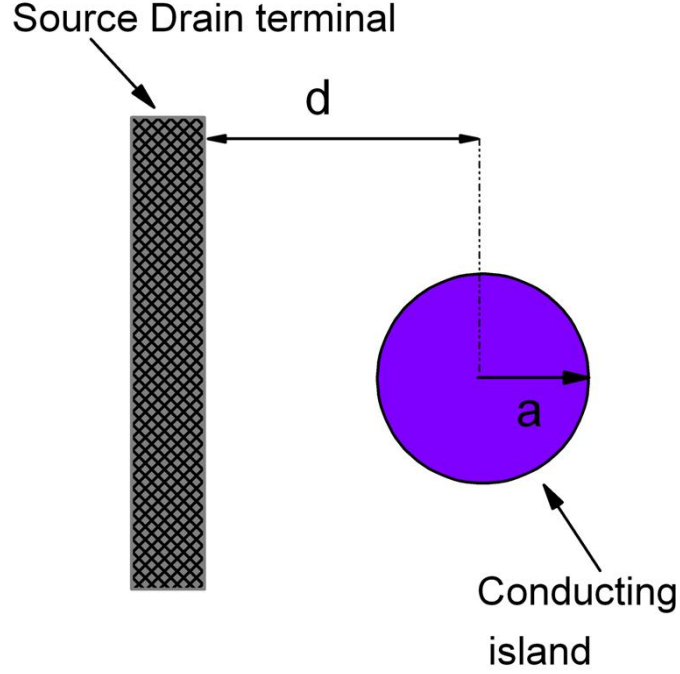
The basic structure of SET is composed of two ultra small tunnel junctions in series and a gate electrode, which is capacitively coupled to the central island. FIB etching was used to fabricate the nano-structures, to realize the tunnel junctions and the central conducting island of the SET device. The SET device was fabricated on a silicon (100) substrate, to insulate the device a thin film of  $Al_2O_3$  having a thickness of 300nm is deposited on silicon, any insulating material can be used instead of  $Al_2O_3$ . A thin metal layer of thickness 8nm of Al or Ni was deposited for the fabrication



of the metal electrodes and the conducting nano-island on the insulating film. The minimum width possible with FIB etching with Hitachi FB-2000A system was 20nm, hence the tunnel junctions were made have a width close to 20nm. The capacitance of the device depends on the geometry of different elements of the device. Assuming the dimensions of the tunneling gaps to be 20nm, the distance between the gate terminal and the conducting island to be 20nm, and the diameter of the spherical conducting island is found to be 45nm, the over all capacitance of the device can be calculated using the classical electrostatics considering the gate terminal to be an infinite metal sheet and the nano-island is separated by a fixed distance.. The conducting island is spherical in shape, and it is embedded in the dielectric material of  $Al_2O_3$ , the capacitance of the island is given by  $C = 4\pi\epsilon\epsilon_r r$  Where  $C$  is the capacitance,  $\epsilon_r$  is relative dielectric constant of the material, and  $r$  is the radius of the conducting island. The capacitance value obtained for the island is  $C_{island} = 0.246aF$

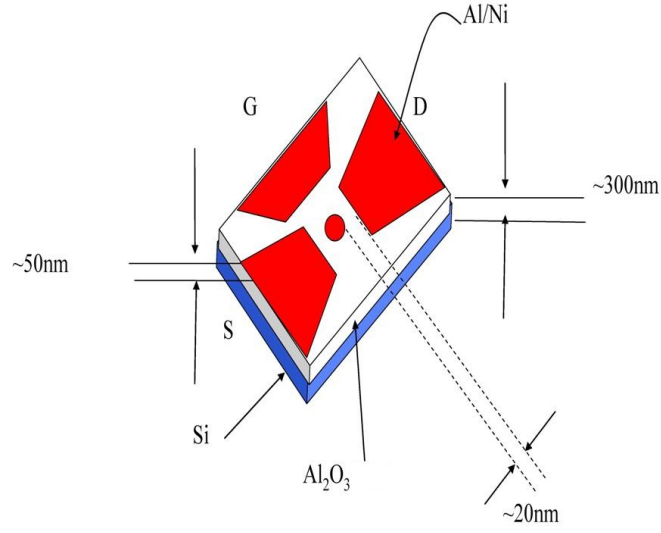
The tunnel junction is composed of a plane of metal on one side and a conducting island on the other side, as shown in Figure 2.12. The capacitance for such a structure is given by [57], the capacitance is calculated based on the electrostatics of the system, assuming that the metal sheet is infinite and the conducting metal island is separated by a fixed distance.

$$C = 2\pi\epsilon\sqrt{d^2 - 4a^2} \sum [coth[(j + 1/2)arccosh(d/2a)] - 1], \quad (2.5)$$



**Figure 2.12:** Capacitance between island and terminal.

where  $a$  is the radius of the sphere, and  $d$  is the distance between the center of the sphere and the metal sheet, considering the gate terminal to be a plane sheet (The geometry is slightly different), the capacitance between the gate and the island is again equal to the capacitance of the tunnel junction. The approximate value of the capacitance of the device is the sum of all the capacitances, and the parasitic capacitances, which are not included here. The calculated capacitance values are shown in Table 2.2. Based on the above calculations of the capacitance of the device, the island size is targeted to have a diameter of less than 50 nm. and the spacing between the island and the source drain terminals is targeted to be less than 20nm, the spacing between the gate and island is also less than 20nm. The above conditions



**Figure 2.13:** Design of SET using FIB etching.

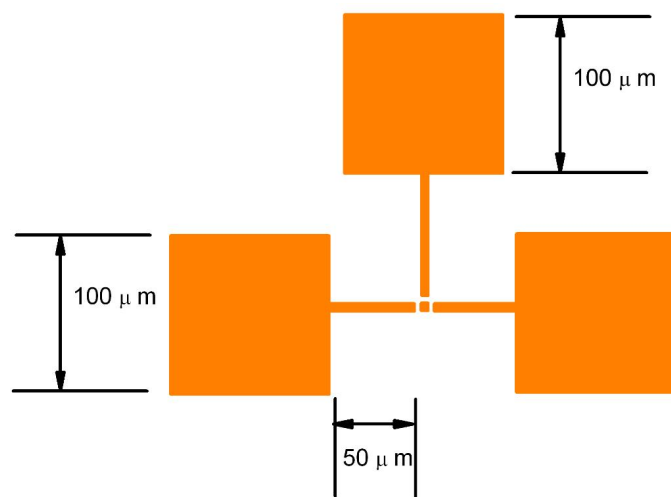
ensures the operation of the fabricated SET device to operate at room temperature. For connecting the device to the external probing pads the source drain terminals have a length of  $50\mu m$ , and a width of  $50nm$ . The gate terminal is having a length of  $70\mu m$  and a width of  $50nm$ . The probing pads have the dimensions of  $100\mu m \times 100\mu m$ . The pictorial view of the device structure is shown in Figure 2.13.

**Table 2.2:** Capacitance calculations

Parameter	Value
$a$	25.0 nm
$d$	20.0 nm
$C_{Tunneljunction}$	$0.104aF$
$C_{Total}$	$0.558aF$

### 2.3.2 SET based on FIB Deposition

The important requirements for the room temperature operation of SET as mentioned before are the small island size, coupled with high tunnel resistance of the tunnel junctions. The entire structure is fabricated using FIB deposition. The active area of the device is made up of nano-electrodes for the source, drain and gate terminals. These active electrodes are connected to the probing pads of the device. The length of the connecting electrodes was  $50\text{ }\mu\text{m}$ , a thickness of 250nm. The nano-electrode connecting the gate probing pad was  $55\text{ }\mu\text{m}$ . The source, drain and gate probing pads are fabricated using FIB deposition. The pictorial view of the device is shown in Figure 2.14. The FIB deposited SET was fabricated using tungsten nano-islands and tungsten trioxide as the tunnel junction material, because of the barrier height for the tunnel junction obtained for the material was high enough to result in large tunnel resistance of the junction. The probing pads and the connecting nano-leads can also be fabricated, using technologies capable of producing features of tens to hundreds of nm in dimensions.

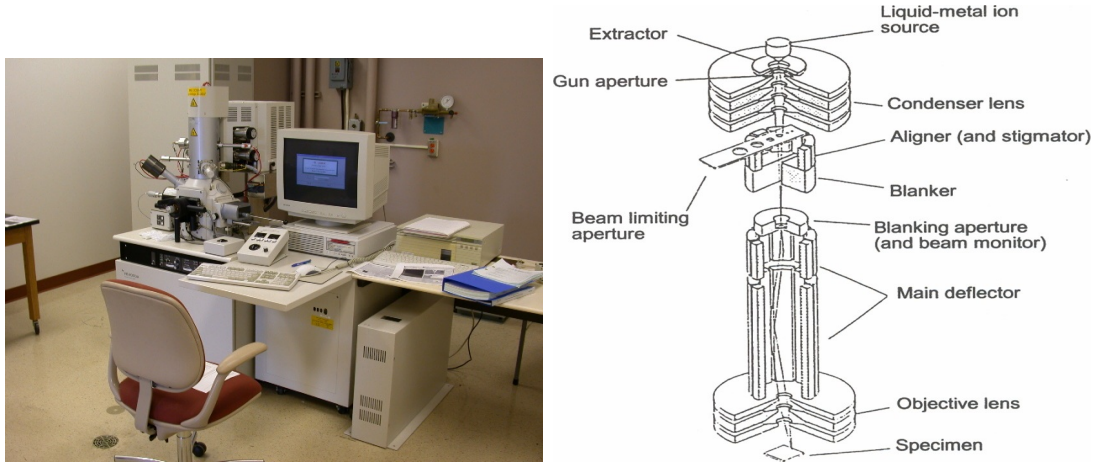


**Figure 2.14:** Design of SET using FIB Deposition.

## Chapter 3

# Fabrication of Single Electron Transistors

Focused Ion Beam (FIB) is utilized in the realization of room temperature operating Single Electron Transistors (SET). Both the FIB etching and FIB deposition were investigated for the fabrication of SET devices. The limitations of the FIB etching process restricts the size of the fabricated nano-structures to  $\sim 40$  nm, and hence makes this method unsuitable for the realization of room temperature operating SET devices [55]. The capability of the FIB deposition process on the other hand allows for the realization of nano-structures in the range of sub 10 nm, and hence the room temperature operating SET devices. The present chapter explains the FIB etching and deposition processes and the development of process technologies for the realization of room temperature operating SET devices using FIB technologies.



**Figure 3.1:** Hitachi FB-2000A Focused Ion Beam System and the exploded view of the FIB column [56] .




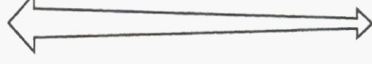
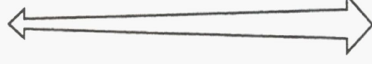
### 3.1 Focused Ion Beam Technology

Focused Ion Beam (FIB) technology has proven to be a very useful tool in the fabrication of nano-scaled structures [58], [59]. This chapter discusses the FIB technology in general and will discuss the capabilities of FIB etching and deposition towards the fabrication of nano-structures [60]. Fabrication technologies realizing reliable and accurate device structures in the nano regime are becoming indispensable, with the reduction of device dimensions. FIB systems have been increasingly utilized in the past decade, mostly for circuit modifications and failure analysis in semiconductor industry [61]. FIB systems are similar to scanning electron microscopes (SEM) in operation, but use focused beams of  $Ga^+$  ions. FIB systems can selectively modify the surface of the sample, and can be used to image the sample surface. The basic features of the FIB system are shown in the Figure 3.1.

The  $Ga^+$  ion beam descending through the FIB column, interacts with different electromagnetic lenses and apertures before scanning the surface of the specimen. The  $Ga^+$  ions are extracted from the liquid metal ion source(LIMS) using an extractor electrode. The gun aperture controls the convergence angle of the ion beam, and the condenser lens controls the beam diameter. The beam limiting aperture selects the required aperture and, hence, the beam current. The other deflectors and lens are used to align the beam on to the sample surface. The Hitachi FB-2000A system has different selection of beams available. Different beams have different beam diameters and different beam currents. The higher the beam number the higher the beam diameter as shown in Figure 3.2. The Hitachi FB-2000A system has beams which can be used in different modes, the beams when used in mode 1 are the milling beams and the beam when used in mode 0 are the observation beams. Most of the processing is done with the beams in mode 1. The milling beams are represented as MI-500 to MI-6 and the observation beams are MO-50 to MO-6 [62]. Beam currents range from 1.0 pA–20.0 nA depending on the beam selected. An Accelerating voltage of 30 kV is possible on the Hitachi FB-2000A system.

The micro structures required for the device fabrication were fabricated using higher beams having higher beam current and the nano-structures can be fabricated using the beams with lower beam current. For the fabrication of device structures, both the beams could be used, depending on the dimensions of the fabricated structure. Higher beam currents, damage the sample surface more than the lower beam currents. Higher



Lens Mode & Aperture	Mode 1 :								
	500	300	200	100	50	20	6	$\mu\text{m}$	
	Mode 0 :								
						50	20	6	$\mu\text{m}$
Beam current	High								Low
Processing speed	Fast								Slow
Resolution	Low								High
SE signal	Strong								Weak
Image roughness	Little								Much

*From: Hitachi FB-2000A, FIB reference manual*

**Figure 3.2:** Hitachi FB-2000A Focused Ion Beam System Beam properties

beam currents are suitable for fabricating micro structures. Lower beam currents are suitable for nano-structures, where high resolution is required for fabrication. Figure 3.3, gives different beam currents and their main application in the processing with FIB. The present chapter deals with the fabrication technologies of the SET using FIB. In the fabrication of SET both the effects of FIB etching and FIB deposition are studied and the process requirements were investigated. The chapter is divided into parts dealing with FIB etching and then FIB deposition.

## 3.2 Focused Ion Beam Etching

The fabrication of SET devices using FIB etching will be presented in this section. A novel nano-fabrication method, which uses the FIB direct write technique to realize

Beam Name	Lens Mode	Aperture Diameter	Indicated Beam Current	Main Usage
L.Scan				Low-mag observation
M1-500	Mode 1	500 $\mu\text{m}$	11.0—15.0 nA	Coarse processing
M1-300	Mode 1	300 $\mu\text{m}$	4.0—8.0 nA	Coarse processing
M1-200	Mode 1	200 $\mu\text{m}$	2.0—3.5 nA	Coarse/medium processing
M1-100	Mode 1	100 $\mu\text{m}$	0.400—0.800 nA	Medium processing
M1-50	Mode 1	50 $\mu\text{m}$	0.100—0.300 nA	Finish processing
M1-20	Mode 1	20 $\mu\text{m}$	0.015—0.040 nA	Finish processing
M1-6	Mode 1	6 $\mu\text{m}$	0.001—0.005 nA	Observation
M0-50	Mode 0	50 $\mu\text{m}$	0.020—0.050 nA	Finish processing/observation
M0-20	Mode 0	20 $\mu\text{m}$	0.004—0.010 nA	Observation
M0-6	Mode 0	6 $\mu\text{m}$	0.000—0.002 nA	Observation

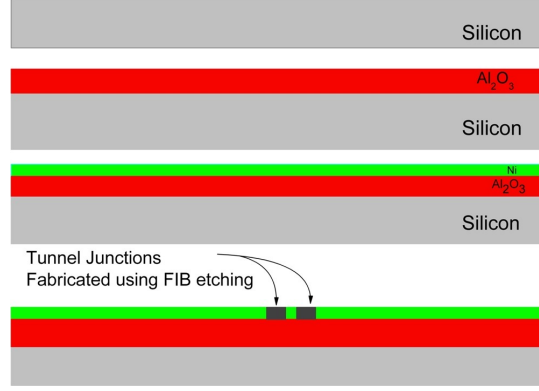
**Figure 3.3:** Hitachi FB-2000A Focused Ion Beam System Beam details

SETs.  $\text{Al}_2\text{O}_3$  is used for tunnel junctions and Ni for conducting islands, measuring pads, and connecting electrodes. The position of the tunnel junctions and the conducting island play a vital role in the characteristics of the device. The present technique allows for precise placement of the tunnel junctions and the conducting island at the required locations, thus enabling the accurate reproduction of the device structure and the device characteristics.

SET devices were fabricated on a lithographically patterned Ni structure. The source, drain, and gate measuring pads for the device were isolated using ion beam etching with high beam current, and the nano-scaled connecting electrodes were fabricated using ion beam etching with low beam current. The active device was fabricated in the final processing step where tunnel junctions and the conducting island were

directly written in the Ni structure. The tunnel junctions had a width of 20nm and the conducting islands a diameter of 49nm. The uniform repeatability of nano-scaled features makes the FIB direct write technique a suitable candidate for the realization of high density integrated circuits and memory. SETs were fabricated in a series of process steps utilizing high beam currents and low beam currents available on the FIB system. The active area of the SET device was made up of a central conducting island, separated from the source and drain terminals via the tunnel junctions. The SET device consists of nano-structures for the active area and micro structures for the connecting leads and probing pads. The etching capabilities of the beam on the FIB system are directly proportional to the energy contained in the beam used. Hence the processing requirements for different structures in the device are different. The nano-scaled features require lower beam currents for processing and the micro to nano interconnecting leads require higher beam currents for processing, and the micro scaled probing pads for the device require higher beam currents for fabrication. The SET device was fabricated on a metal thin film (Al or Ni) of 50nm, which was deposited on an insulating layer of  $Al_2O_3$  having a thickness of 300nm. The insulating layer was deposited on silicon substrate.

The process flow for the fabrication of SET by FIB direct write technique is shown in the Figure 3.4. A silicon wafer is diced into samples of size 0.5 cm  $\times$  0.5 cm using the dicing saw instrument, the silicon samples were thoroughly cleaned in piranha solution, and then rinsed in DI water. The cleaned samples were introduced into



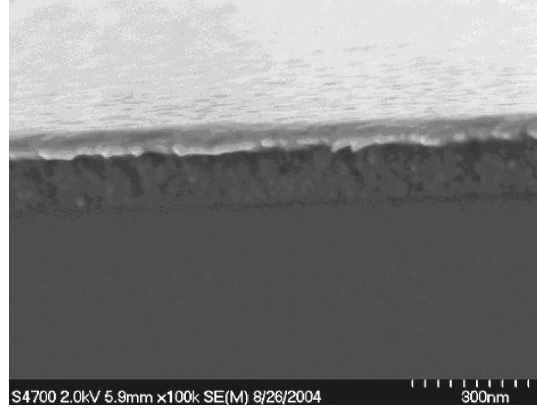
**Figure 3.4:** Process flow for the fabrication of SET with FIB etching.

the Perkin Elmer 2400-8J parallel plate sputtering system for the deposition of oxide and metal layers. When the chamber pressure reaches in the range of  $10^{-7}$  Torr, the sputtering of oxide film is initiated. A 300nm thin film of  $Al_2O_3$  is deposited on the introduced clean silicon wafer. Following the deposition of  $Al_2O_3$ , without changing the vacuum conditions in the process a 8nm thin layer of Nickel (Ni) was deposited using the same system. The deposition conditions for both the thin films in the sputtering system are summarized in the Table 3.1. For the deposition of  $Al_2O_3$ , the  $Al_2O_3$  target was used in the sputtering chamber. For the deposition time of 30 minutes, the resulting thickness of the Ni thin film was 50 nm. It was observed that the above deposition parameters resulted in good quality thin films. The cross section of the sample containing the stack of thin films is clearly shown in the SEM micrograph of Figure 3.5.

Samples having the thin film stack of  $Al_2O_3$  and Ni were thoroughly cleaned and introduced into the photoresist spinner. Because the sample size was small, an

**Table 3.1:** Process parameters for the deposition of thin films in 2400-8J parallel plate Perkin Elmer system

Process Parameter	Material 1	Material 2
Deposition Material	$Al_2O_3$	Nickel
RF Power	900 W	650 W
DC Bias	-451 V	-463 V
Substrate Bias	0 V	0 V
Process Pressure	9.6 m Torr	5.7 m Torr
Gas Flow	Ar: 14.0 SCCM, O2: 2.0 SCCM	Ar: 7.0 SCCM
Substrate Temperature	Room temperature	Room temperature
Deposition Time	30 minutes	30 minutes

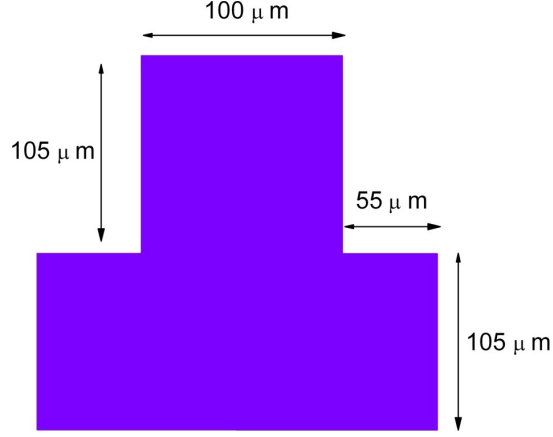


**Figure 3.5:** SEM micrograph of the Cross section of the deposited thin film stack using Perkin Elmer 2400-8J sputtering system.

extended holding chuck for the wafer was used to load the samples in the spinner.

A thin layer of photoresist was spun at a speed of 3000 rpm. The top Ni thin film layer is lithographically patterned to obtain structures in the shape of an inverted “T” having the dimensions as shown in the Figure 3.6. The patterned Ni tin film was thoroughly cleaned and dried in nitrogen ambient.

Samples having these Ni patterns are introduced in the Hitachi FB-2000A FIB system



**Figure 3.6:** Lithographically patterned Ni thin film.

for further processing to fabricate the SET device and the measuring pads of the device. The source, drain, and gate measuring pads, with the connecting leads and the active device, consisting of the conducting island and the tunnel junctions are fabricated using FIB direct writing on the lithographically patterned Ni structure. Fabrication of any pattern with the FIB requires a CAD image file of the pattern to be fabricated, which can be generated using the on board software with the Hitachi FB-2000A FIB system. The beam raster scans the sample surface, following the CAD pattern. In order to write the pattern on the sample surface. The direct writing on the sample with FIB depends on the following process parameters:

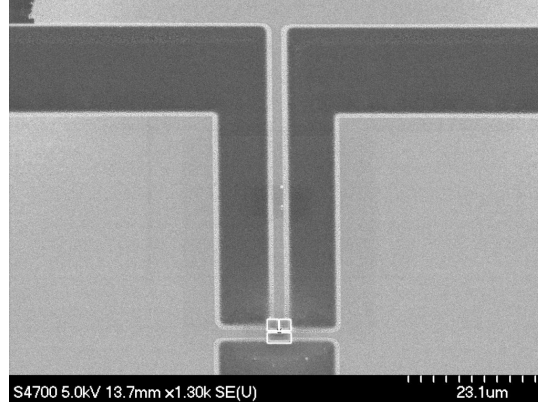
- † The beam used, dictates the amount of energy imparted to the pixels. The selected magnification area on the sample surface (higher magnification area requires beams with higher beam current and the smaller magnification area requires beams with lower beam currents for processing).

† The dwell time used for the processing, which is the time the ion beam spends on each pixel of the required pattern.

† The frame number, which is the number of iterations the beam dwells on each pixel.

Fabrication of different structure (micro and nano-structures) using FIB etching on the device requires selective etching of the thin film (Ni in this case). Among the different beams available on the Hitachi FIB system, it was observed that beams with a higher beam number, such as MI-500, reduce the processing time but did not have resolution fine enough to fabricate connecting leads of  $3.0\ \mu\text{m}$  width. On the contrary, the beams with a smaller beam number, such as MO-20, had fine resolution but required longer fabrication times. The beam MI-300, having the beam current of 4.0-8.0 nA, had sufficient resolution to fabricate the connecting leads with a width of  $3\ \mu\text{m}$  and a shorter processing time to isolate the source, drain, and gate terminals. The processing time was about 6 minutes to fabricate the connecting leads which are connected at the center of the active structure, as shown in the Figure 3.7. The macro scaled features of the SET device could be fabricated using standard photolithography and etching processes. Fabrication using the FIB was utilized to further explore the capabilities of the FIB technology.

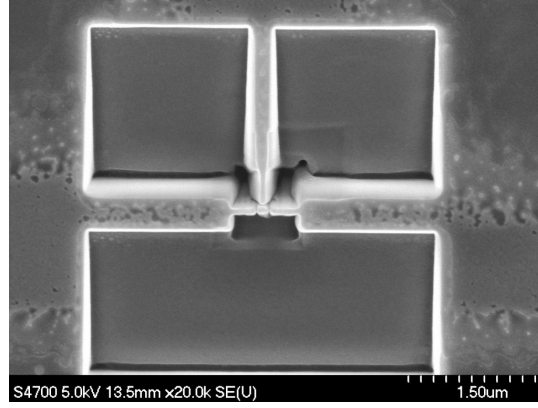
The fabrication of the SET device starts with the fabrication of the micro scaled probing pads which are isolated using the beam MI-300. The magnification area on



**Figure 3.7:** Magnified SEM view showing the active device area of the SET at the center connecting leads.

the FIB is chosen to be  $256 \mu\text{m}$ , after locating the Ni pads fabricated using the lithography process, the etching of the Ni thin film is initiated in order to isolation the probing pads to create the micro scaled connecting leads, formed as the inverted "T" structure. After the fabrication of the micro scaled leads, at the center of the inverted "T" structure a magnification are of  $4 \mu\text{m}$  is selected to initiate the etching process using the beam M0-50. At the center of the inverted "T" structure nano-scaled electrodes are fabricated. The nano-scaled electrodes connect the measuring pads and the active device, which are directly written using the beam MO-50. The SEM micrograph of the fabricated nano scale electrodes are shown in the Figure 3.8. The width of the connecting electrodes was reduced to  $300\text{nm}$  using the beam MO-50. The active device can be seen at the center of the inverted "T" structure, which was fabricated in the processing step following the fabrication of the nano-scaled electrodes.



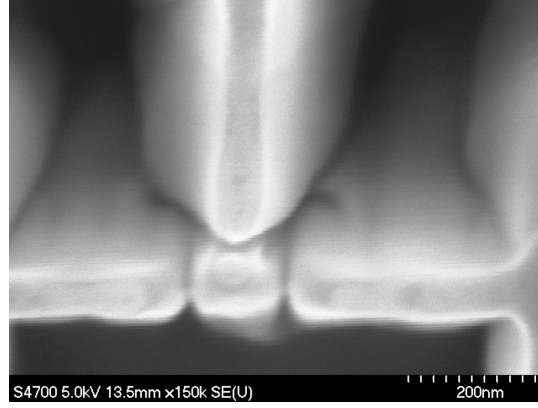


**Figure 3.8:** SET active device structure formation by FIB using progressive ablation and beam focus.

**Table 3.2:** FIB processing parameters for micro and nano scaled structures using FIB etching

Process Parameters	Macro scaled structures	Nano scaled structures
Beam	MI-300	MO-50
Beam current	4.0-8.0 nA	20.0-5.0 pA
Dwell time	128 $\mu$ sec	128 $\mu$ sec
Frame number	50	10
Magnification Area	256 $\mu\text{m} \times 2$	32 $\mu\text{m} \times 8$
Etch time	6 minutes	5.3 minutes

The processing parameters for the fabrication of both the micro scale and nano-scaled, connecting electrodes to the device using FIB processing, are summarized in the Table 3.2. Beam MO-20 is selected and at the center of the inverted “T” structure a magnification area of  $4 \mu\text{m} \times 1$  is selected to further reduce the width of the connecting electrodes to 50nm. The nano pattern generation system (NPGS) software [63], which is an addition to the onboard FIB software having increased pixel density in the generated CAD files, is used to control the scan coils of the FIB to



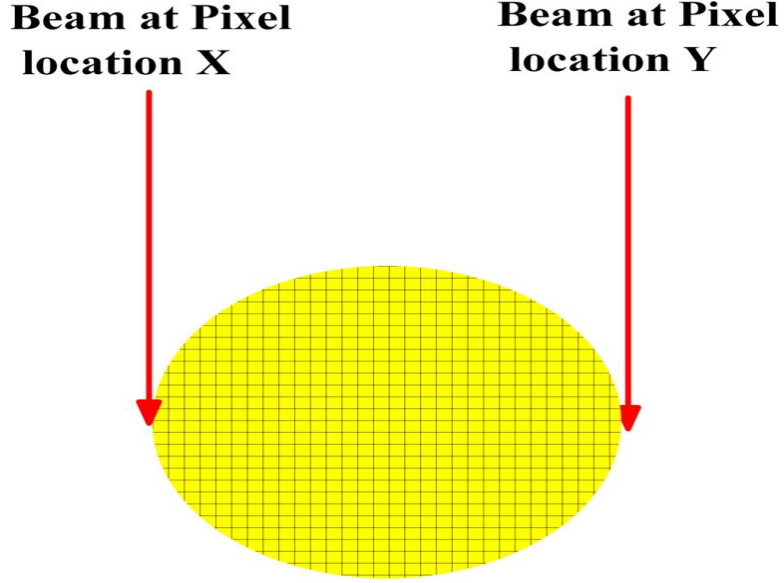
**Figure 3.9:** SEM view of the active SET device showing quantum island definition and localization.

fabricate the nano-scale leads connecting the device. The active device was fabricated at the center of the inverted “T” structure, using the beam MO-6, which has a beam diameter of 10nm and a beam current of 0-2 pA, the selected magnification area was  $4\mu\text{m} \times 4\mu\text{m}$ . The tunnel junctions and the central metallic island were fabricated using the beam MO-6. The tunnel junctions were 20nm wide, and the metallic island was 50nm in diameter, as clearly shown in the Figure 3.9. The position of the tunnel junctions and the position of the conducting island can be precisely controlled to fabricate structures which are repeatable. FIB technology can be used to accurately reproduce the device structures, thus, producing the device characteristics across many devices. The fabricated metallic island at the center of the SET device has the dimensions close to of 45nm. The island structures less than 40nm in diameter are difficult to fabricate using the above explained FIB etching technique. The interaction of the FIB beams are responsible for the limitations seen in the fabrication process, which are explained in detail in the next section.

### 3.2.1 Limitations of the FIB Etching process

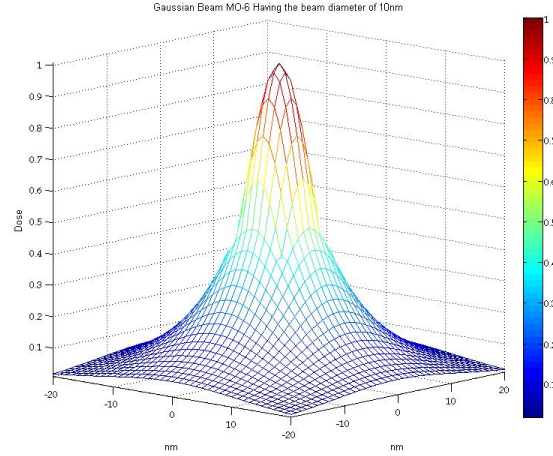
Hitachi FB-2000A FIB instrument is used to fabricate the electrodes and the conducting island for the SET. The FB-2000A has a selection of beams that can be used for milling and observation. The beam MO-6 is an observational beam having the smallest aperture of  $6\text{ }\mu\text{m}$  resulting in a focused beam having a diameter of 10nm on the sample surface [62]. To fabricate an island of given radius,  $r$ , the ion beam raster scans the pixels in the selected magnification area. The numbers of pixels that are illuminated by the ion beam are determined by the selected magnification area, the center to center distance which is the spacing between neighboring pixels and the distance between two raster scans of the beam, is defined as the line spacing. The ion beam dwells on the pixels which are selected by the CAD design of the required circular shape, Figure 3.10. represents two such pixel locations, X and Y, which are separated by a distance equal to the diameter of the required island size.

The dwell time is the time, the beam stays on each pixel. The magnification used on the FIB was 145.000, the distance between the neighboring pixels was  $5.3\text{\AA}$ , the line spacing was  $5.3\text{\AA}$ , and the dwell time used was  $450\text{ }\mu\text{ sec}$  with beam current of 1.0 pA. To fabricate the required island in a Ni thin film having a thickness of 12nm, the pattern was repeated ten times with the same process parameters for each repetition. The pattern repetition helps in imparting a minimum energy dose at a given time to the pixels.



**Figure 3.10:** FIB etching mechanism.

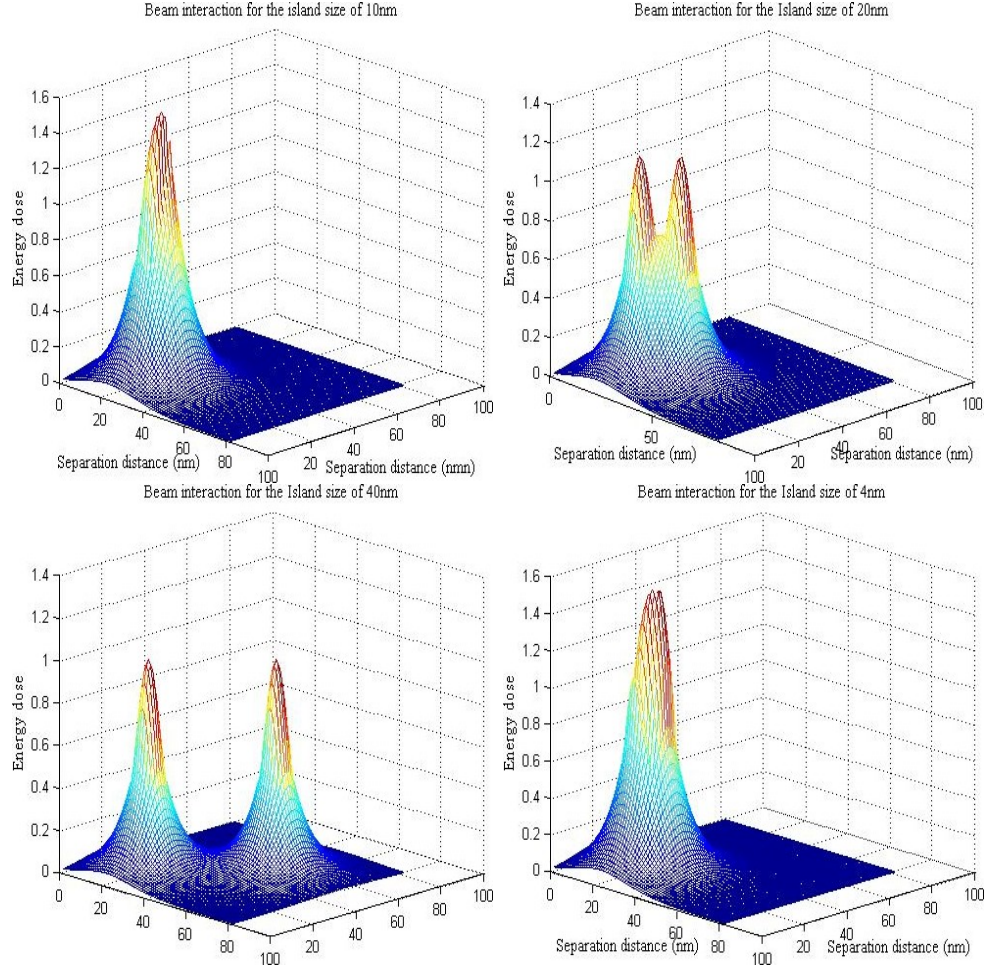
The energy imparted to the pixels is calculated as follows: For a beam of voltage,  $V$ , and current density,  $J$ , the total input power is the product of  $V$ , the current density,  $J$ , and the area of the beam [64], since the current density profile of the beam is Gaussian, the energy imparted to the pixels locations is also Gaussian in nature. The interaction of these beams at different pixels at different times can be thought of as an energy interaction on the surface of the sample. The energy interactions of the beam that is illuminated at the two corners of the diameter (which are parallel pixels) of the fabricated circular shape are considered, the displaced distance between the beams is the diameter of the fabricated island. The displaced distance is varied from 50nm to 4 nm and the modeled interactions of the energy imparted to the pixels on the surface of the sample are studied. The reduction of the diameter of the island results in the overlap of the two beam energies, and the energy overlap increases with the



**Figure 3.11:** Beam profile of the FIB beam.

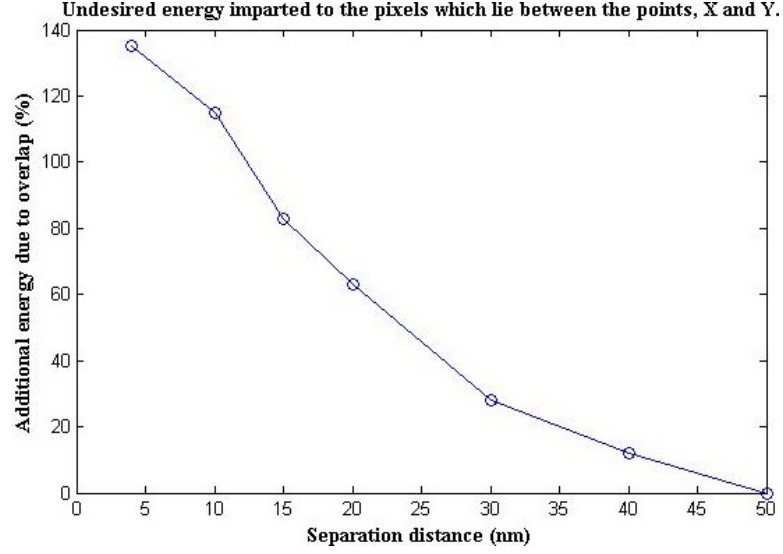
reduction of the diameter of the island. The undesired energy dose imparted to the pixels which lie between the pixels, X and Y, increases with the overlap of the beam energies as shown in Figure 3.11. It can be concluded that the overlap is minimal for the separation of 50nm and hence the energy imparted to the pixels which are between the beams is negligible.

For the islands less than 45nm in diameter, undesired energy is imparted to the pixels which lie inside the island, due to energy overlap. This energy increases rapidly with the reduction of island size. For the separation distance of 20nm the overlap of energies is 63% of the peak beam energy, and increases to 135% of the peak beam energy for a separation distance of 4nm, as clearly shown in Figure 3.13. The percent of overlap of the energy dictates the island size that can be fabricated. Experimental



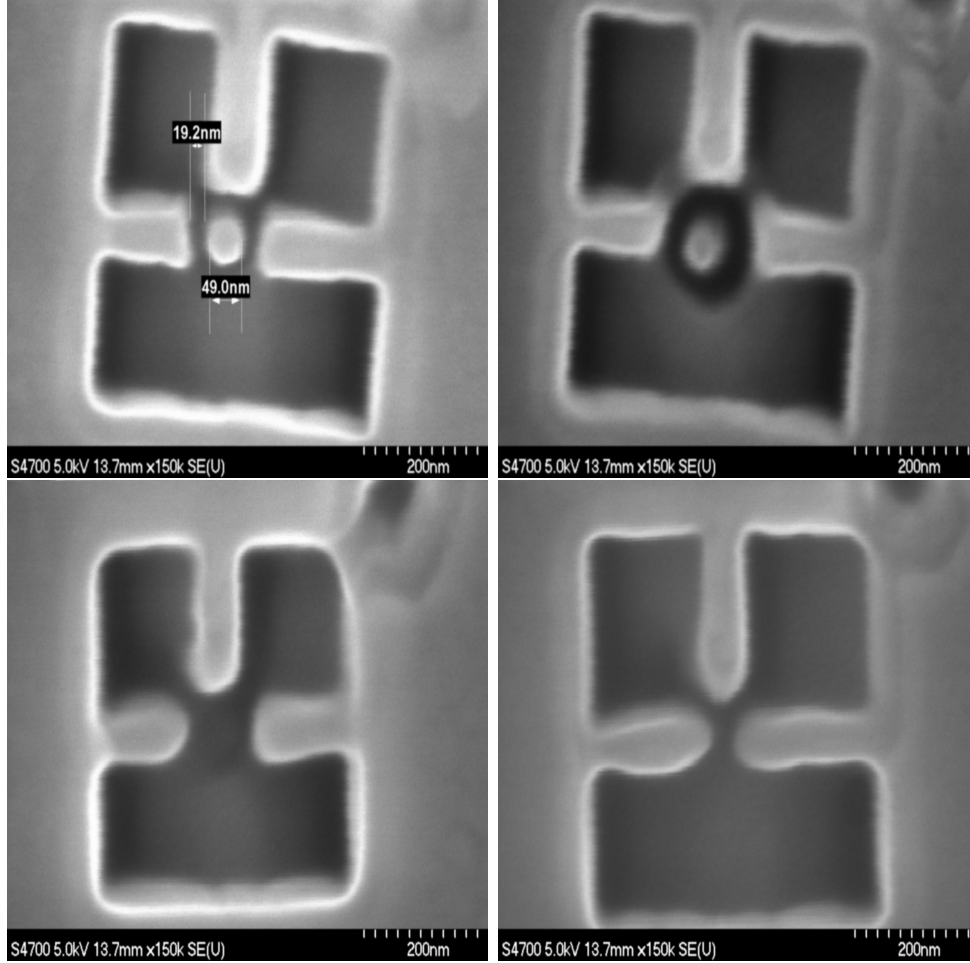
**Figure 3.12:** Energy overlap of FIB resulting from the beam overlap .

results demonstrate the etching of islands less than 45nm in diameter. The SEM micrographs shown in Figure 3.14. clearly reveal the quantum island having a diameter of 49nm and tunnel junctions having a width of 19nm. From both, the modeling of the beam energy interaction and the experimental results, it can be concluded, that quantum islands having the diameter of less than 45nm are etched away, and quantum island having the diameter of 49nm and tunnel junctions having a width of 19nm are successfully fabricated using the FIB etching.



**Figure 3.13:** Percentage of energy overlap.

Because of the limitations of the FIB etching process, nano islands less than 40 nm in diameter cannot be fabricated using the etching technique discussed above. For the room temperature operation of the SET device nano islands having diameters of sub 10 nm are required, Hence alternative methods for the realization of the nano islands have to be investigated. One of the alternative methods to the FIB etching is the FIB deposition which is addressed in the following section.



**Figure 3.14:** SEM Micrographs of the fabricated SET devices.

### 3.3 Focused Ion Beam Deposition

Focused Ion Beam is primarily used in IC fabrication, where the two important applications include the removal of material by micro milling and the deposition of materials using ion induced deposition. FIB is also used in semiconductor industry in applications like failure analysis, defect characterization, design modification, and process control [65]. FIB induced deposition is used to deposit both metal and Insu-



lator materials on the sample surface. The deposition process takes place by means of ion induced chemical vapor deposition (CVD). For the deposition to occur a precursor gas is sprayed on to the sample surface by the deposition nozzle, the sprayed gas is adsorbed on the sample surface and the incident ion beam decomposes the adsorbed precursor gas forming the desired product. The byproducts of the reaction process are a volatile gas which is removed through the vacuum system [66; 67]. In practice both milling and deposition occur simultaneously. The milling of the substrate is suppressed almost completely by suitable selection of scanning parameters to obtain a continuous film [68]. The important parameters in the deposition process are the ion beam current density, the scan speed, the loop time and the scanning strategy of the beam during deposition [69]. Deposition of nano islands can be achieved by the deposition of discontinuous film. This can be achieved by a suitable selection of scanning parameters, which would increase the sputtering effect on the substrate resulting in a discontinuous thin film having the required nanostructure. Dwell time is the time the beam spends on each pixel of the pattern to be deposited. The dwell time of the deposition process can affect the nanostructure of the deposited thin film, and hence should be optimized to obtain the required nano structure. For the deposition of the nano islands of required island size, the dwell time of the deposition process should be optimized to have a dominant sputtering effect while the deposition occurs on the sample surface.

### 3.4 Deposition of nano islands using Focused Ion Beam deposition

In this section the effect of dwell time, ion beam current density and the deposition pattern size on the fabricated nano structure is investigated. It was observed that the fabricated nano structure size depends on all of the above process parameters, and was found to predominantly depend on the dwell time of the process. It is shown through experimentation and theoretical modeling that the deposited island size can be modulated with the dwell time.

Let  $L$ ,  $W$  and  $Z$  be the length, width and height of the deposited thin film using FIB deposition. According to the macroscopic model for FIB induced deposition developed by Overwijk and Heuvel [69], the net deposition rate is the result of the competition between FIB induced deposition and sputtering action of the ion beam. The process parameters of importance in FIB deposition are dwell time, refresh time, spot size, and beam current. In addition, ion dose, vacuum of the chamber, and precursor gas pressure are also essential for deposition process and the dwell time is key parameter for deposition process. Then sputtering process will play a dominant role for higher dwell times [67]. The deposition yield of the FIB deposited film [68] is given by Equ. (3.1).

$$Y_D = \frac{WLZ}{I_B t} \quad (3.1)$$

Where  $I_B$  is the Ion beam current, and  $t$  is the total deposition time. For the fabrication of nano islands the sputtering component of the deposition process should dominate. From the Equation 1 it can be seen that the deposition yield is dependent on the deposited pattern size, the beam current and the total deposition time. The ion beam current can be changed by changing to a different beam for deposition and beams with higher beam current will have an effect of lowering the deposition yield of the deposited thin film. The other parameter of interest that reduces the deposition yield is the total deposition time of the process. For a fixed deposition pattern the length and width of the deposited pattern is fixed. Consider a pattern having length  $L$  and width  $W$ , for the deposition to occur the given pattern is divided in to fixed number of pixels, let  $n_1$  and  $N_2$  be the number of pixels along the length and width of the given pattern. The beam dwells on each pixel, and the time taken by the beam to cover all the pixels in the pattern to be deposited once is known as the loop time. In one loop time the beam dwells on each pixel and also spends time in between the pixels when it moves from pixel to pixel. Let the time the beam spends on each pixel be  $t_d$  which is the dwell time of the process and the time spent by the beam between the pixels be represented by  $t_{bp}$ . If  $n_1$  and  $N_2$  be the number of pixels, then  $n_1 - 1$  and  $n_2 - 1$  will be the number of spaces in between the pixels as shown in Fig 1. The total number of pixels where the beam dwells on the pixels is  $n_1 N_2$  and the number

of available spaces are  $n_1 - 1$ ,  $n_2 - 1$ . Neglecting the beam blanking time, the loop time of the deposition process is then equals to the time spent on each pixel and the time spent between the pixels. The loop time is then given by Equ. (3.2)

$$t_1 = n_1 n_2 t_d + (n_1 - 1)(n_2 - 1)t_{bp}. \quad (3.2)$$

The total deposition time is then given by the product of the loop time and the number of loops involved in the deposition process as given by the Equ. (3.3) . The interlace of the deposition process is a parameter that controls the spacing between the adjacent pixels, and thus controls the irradiation interval of the beam. The larger the interlace, larger would be the distance between the adjacent pixels. Interlace is typically set at lower values for normal deposition to obtain a uniform thin film during FIB deposition. With the increase in the interlace value the time spent by the beam in between the pixels increases. Knowing the dwell time and the loop time, the time spent by the beam in between the pixels can be obtained from the Equ. (3.2). Hence the total deposition time can be written as

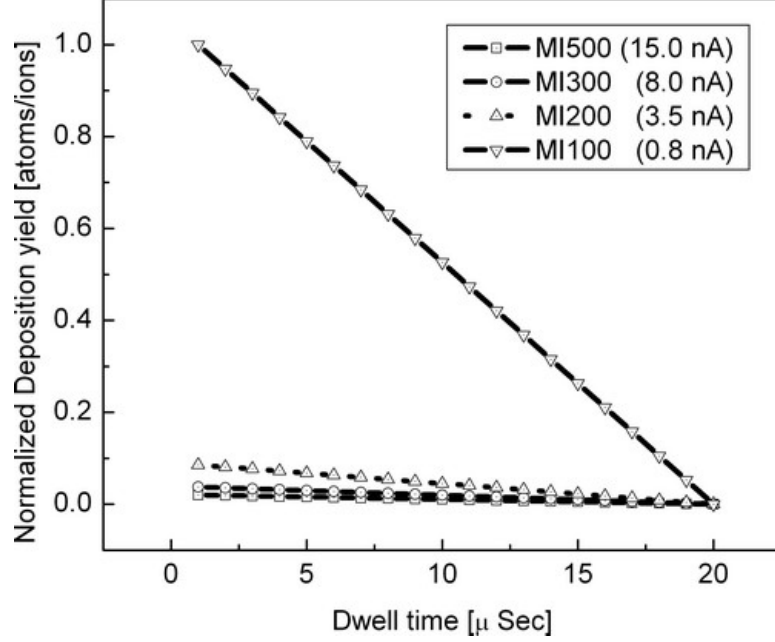
$$t = n_1 [n_1 n_2 t_d + (n_1 - 1)(n_2 - 1)t_{bp}] \quad (3.3)$$

Incorporating the effect of dwell time in the total deposition time the deposition yield of the deposited film for a fixed pattern size and for a fixed beam current can be

written as

$$Y_D = \frac{WLZ}{I_B n_l [n_1 n_2 t_d + (n_1 - 1)(n_2 - 1)t_{bp}]} \quad (3.4)$$

Where  $n_1$  is the number of loops of the deposition process which can be calculated  $n$  from the total deposition time and the loop time of the process. It can be concluded from Equ. (3.4) that the deposition yield can be controlled by varying the dwell time of the deposition process for a fixed pattern size and a for a given beam current. The higher the dwell time the lower the deposition yield and visa versa. The theoretical dependence of the different process parameters like the beam current and the dwell time of the deposition process are summarized as the normalized deposition yield obtained from the simulations in the Figure 3.15. The deposition yield decreases with the increase in the beam current, the normalized deposition yield decreases with the increase in the beam current from 15.0 nA to 0.8 nA (beam MI 500 to beam MI 100).

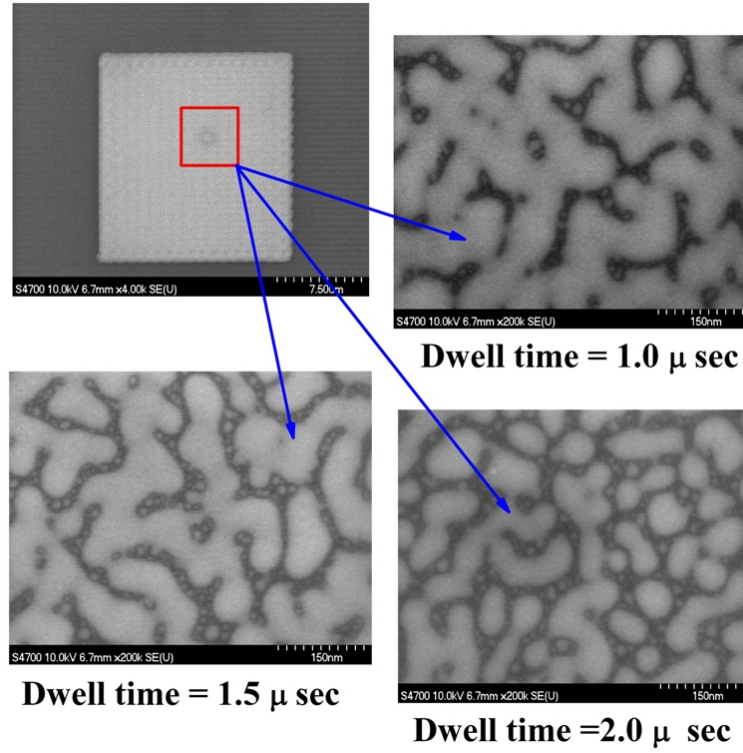


**Figure 3.15:** Variation of deposited nano structure with increase in dwell time

### Experimental Verification

Tungsten pads having dimensions of  $16.062 \mu\text{m} \times 16.062 \mu\text{m}$  was deposited on a 300nm thick  $\text{Al}_2\text{O}_3$  present on a silicon wafer. The  $\text{Al}_2\text{O}_3$  was sputter deposited using Perkin Elmer 2400-8J, RF sputtering instrument. The silicon wafer with  $\text{Al}_2\text{O}_3$  was thoroughly cleaned in Piranha solution, which is a solution having a 1:1 volume ration of  $\text{H}_2\text{SO}_4$  and  $\text{H}_2\text{O}_2$ , for five minutes. The samples were then rinsed in de-ionized water and dried in nitrogen environment. The cleaned samples were introduced in to the Hitachi FB-2000A Focused Ion Beam system. The process pressure in the FIB chamber would be in the range of  $1 \times 10^{-6}$  Torr while the deposition was in progress. The  $\text{W}(\text{CO})_6$  is used as a precursor gas for the deposition of tungsten. Hitachi FB-

2000A FIB system, has a different selection of ion beams which can be used for the processing. From the selection of beams the beam MO-200, having a beam current of 0.8 nA and beams with lower beam current than MO-200 are typically used for the deposition of tungsten thin films. To increase the sputtering effect during the deposition process the beam MI-200 having a beam current of 3.5 nA was selected for the deposition. The interlace is fixed at 8.0 which is maximum value on the Hitachi FB-2000A instrument. The larger interlace will increase the time spent by the beam in between the pixels. The deposition of tungsten was carried out for different dwell times of 1.0  $\mu$  sec 1.5  $\mu$  sec and 2.0  $\mu$  sec. The deposited thin films were examined for the changes in the nano-structure of the deposited thin films for the variation in the dwell times of the beams; the effect of dwell time on the deposited nano-structure is shown in SEM micrograph of Figure 3.16. The dwell time of the deposition process was varied from 1.0  $\mu$  sec to 8.5  $\mu$  sec for a total deposition time of 0.1 minutes. The fabricated nano-particles for different dwell times are shown in the Figure 3.17. The fabricated pattern size is reduced to 10.062 $\mu$ m to study the effect of reduction in the pattern size. The dwell time of the deposition process was varied from 1.0  $\mu$  sec to 15.0  $\mu$  sec for a total deposition time of 0.1 minutes. The STM micro graph of the deposited nano particles on gold thin film is shown in Figure 3.18. The nano particles are shown to have a height of 3nm.

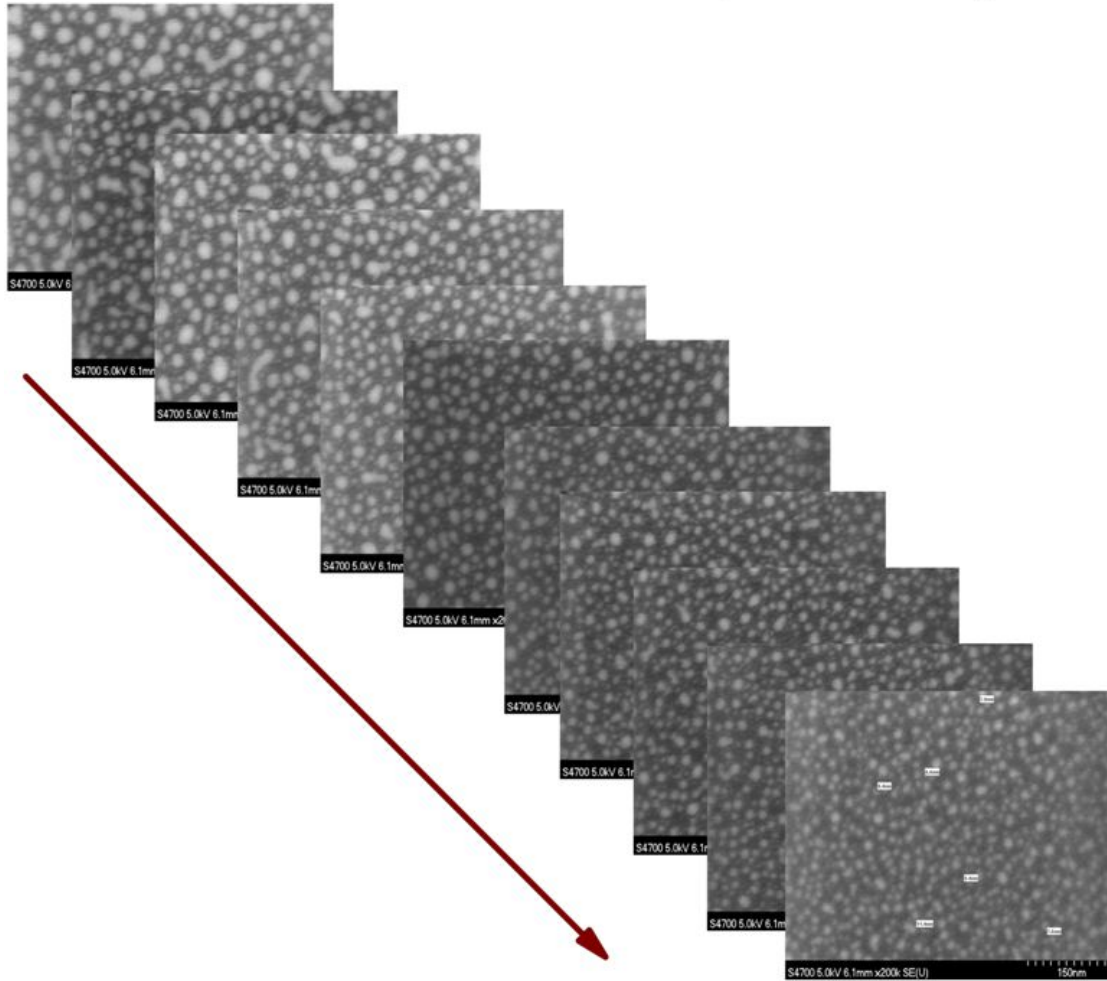


**Figure 3.16:** Variation of deposited nano structure with increase in dwell time

In order to study the effect of variation in the beam current the beam MI 100 having a beam current of 0.8 nA was used for the deposition of tungsten. The size of the deposited structure was fixed at  $10.062 \mu\text{m} \times 10.062 \mu\text{m}$  and the dwell time was changed from  $1.0 \mu\text{sec}$  to  $15.0 \mu\text{sec}$  and the resulting nano-structure was observed under SEM. The SEM micrographs of the fabricated nano-islands for variation in the dwell times are shown in Figure 3.19. The variation in the deposited pattern size was reduced to  $5.062 \mu\text{m} \times 5.062 \mu\text{m}$ , to study the deposited pattern size dependence with the dwell time. The deposition yield can be controlled by the variation in the size of the deposited structure and is directly proportional to the size of the deposited



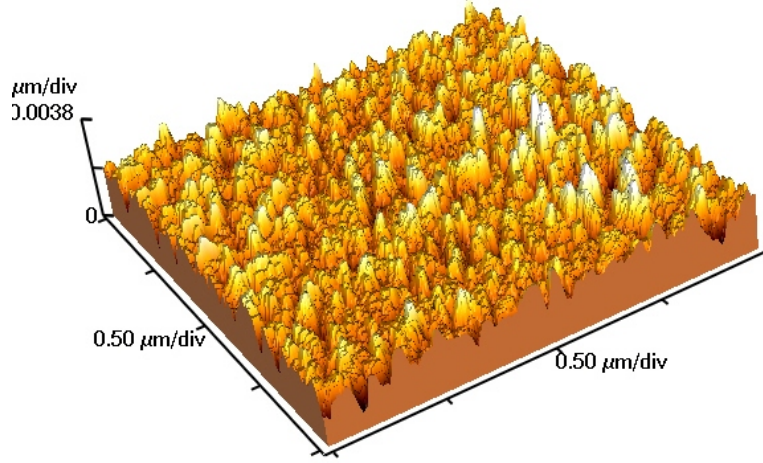
**Dwell time increased from 3.0  $\mu$  s to 8.5  $\mu$  sec**



**Island size decreased from 30 nm to 8.5nm**

**Figure 3.17:** Variation of deposited nano-island size with increase in dwell time of MI200

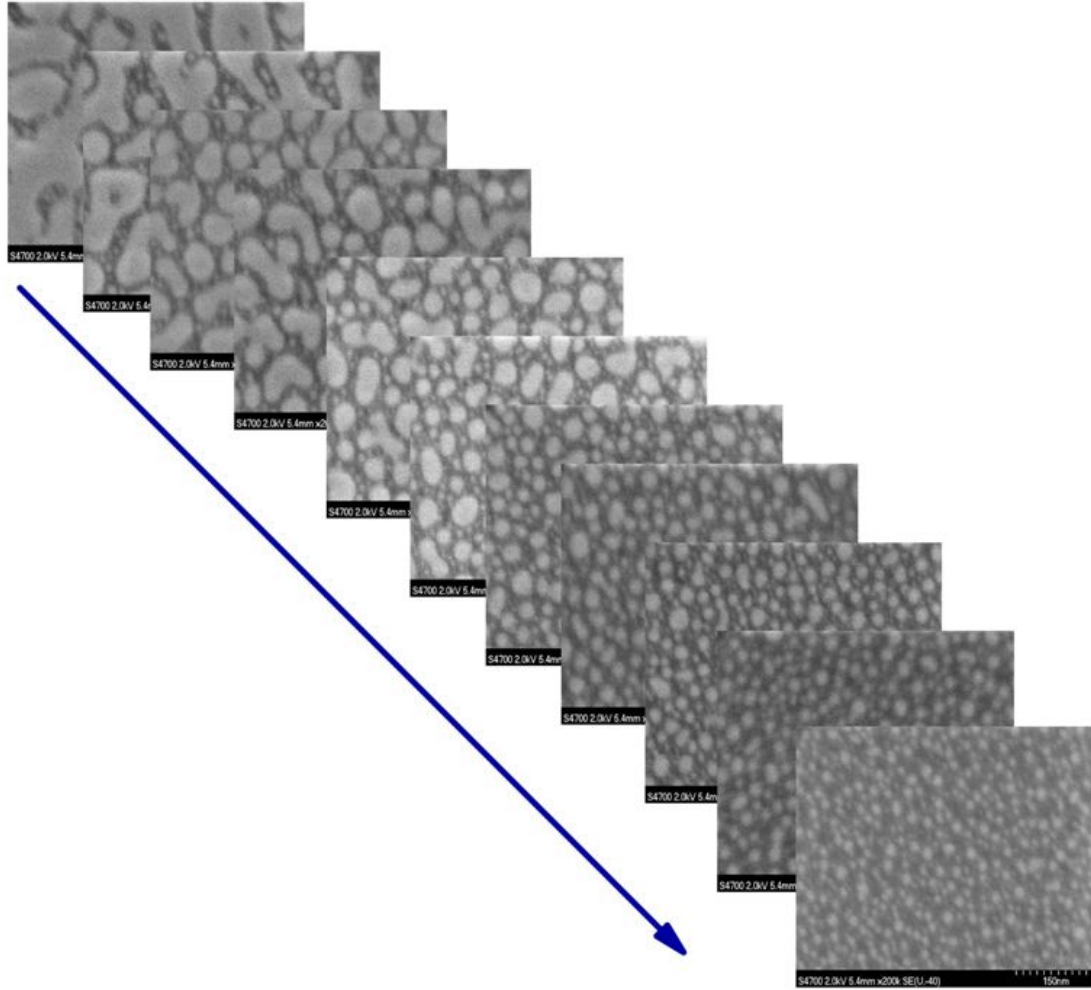
structure, and inversely proportional to the beam current and the total deposition time. Figure 3.20 shows the effect of increase in dwell time on the deposition yield for a different beam current (MI100). The deposition yield decreases with the increase in the dwell time of the process.



**Figure 3.18:** STM micrograph of the fabricated nano particles on gold substrate

From the obtained nano-structures of the deposited thin film, the average nano-structure size was plotted against the dwell time of the deposition process. The deposition yield is proportional to the fabricated island size, and hence the island size is plotted against the variation of dwell time and the beam current. It can be seen that the average island size can be controlled by the dwell time of the process. The dependence of the fabricated island size on the dwell time and the size of the patterned structure is summarized in the Figure 3.21. for the patterned structure of  $16.062\mu\text{m} \times 16.062\mu\text{m}$  the deposited island size decreases from 30nm to 8nm for a dwell increase from  $3.0\mu\text{ sec}$  to  $8.0\mu\text{ sec}$ , and for the patterned structure of  $10.062\mu\text{m} \times 10.062\mu\text{m}$  the island size decreases from 100nm to 8nm for an increase of dwell time from  $1.0\mu\text{ sec}$  to  $15.0\mu\text{ sec}$ . Increase in the dwell time of the process increases the sputter yield of the process, thereby decreasing the deposition yield, resulting in

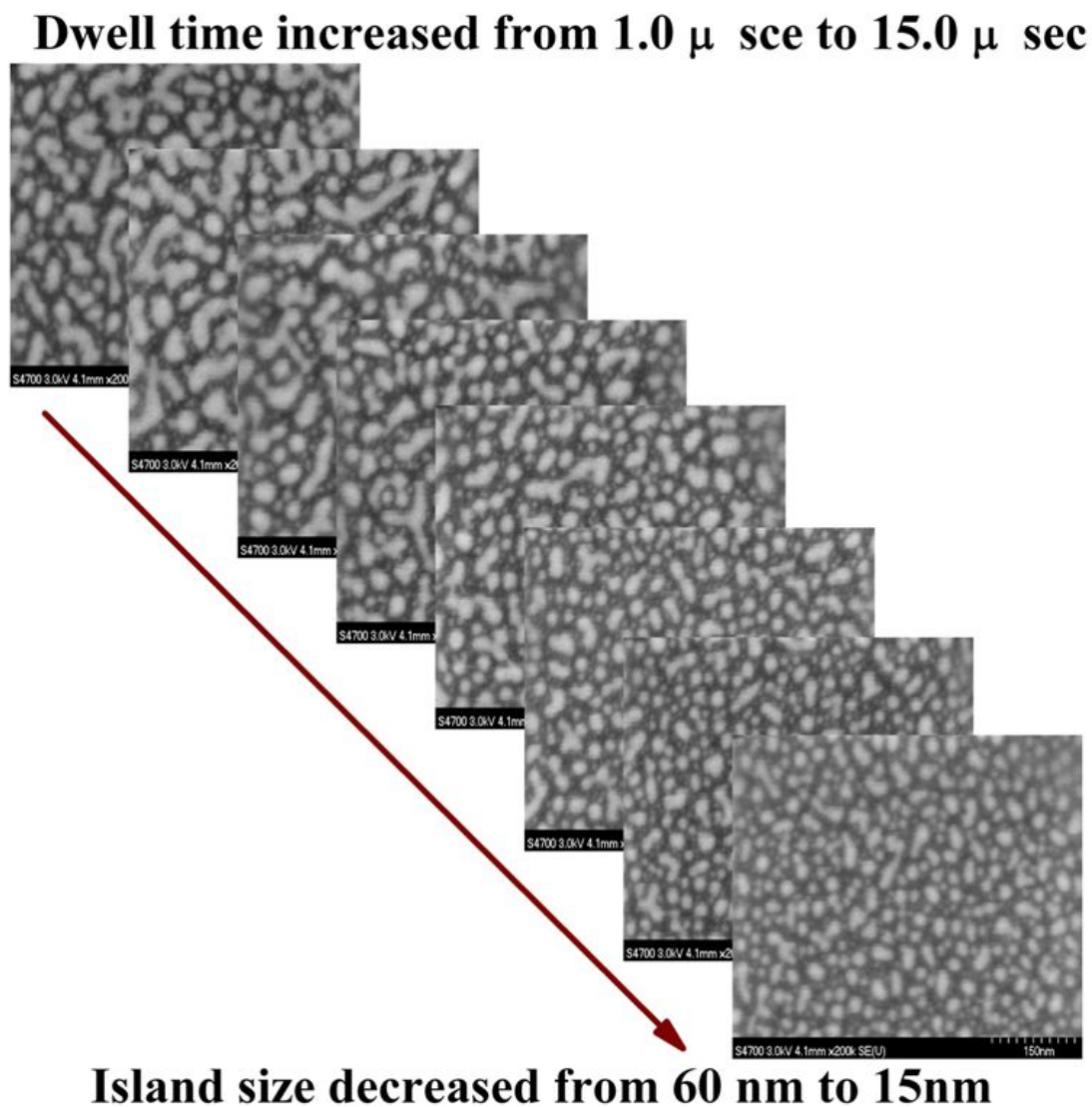
**Dwell time increased from 1.0  $\mu$  sec to 15.0  $\mu$  sec**



**Island size decreased from 50 nm to 10nm**

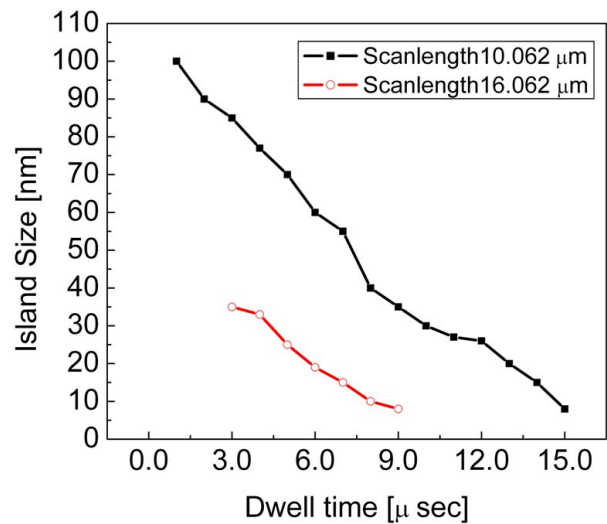
**Figure 3.19:** Control of island size with beam MI200

reduction of the deposited island size. The increase in the deposited structure size reduces the deposited island size because the increase in the structure size would increase the distance between the pixels, thus increasing the time spent in between the pixels, which reduces the deposition yield. The number of pixels in the selected area are fixed by the scanning software on the FIB instrument. With the increase in

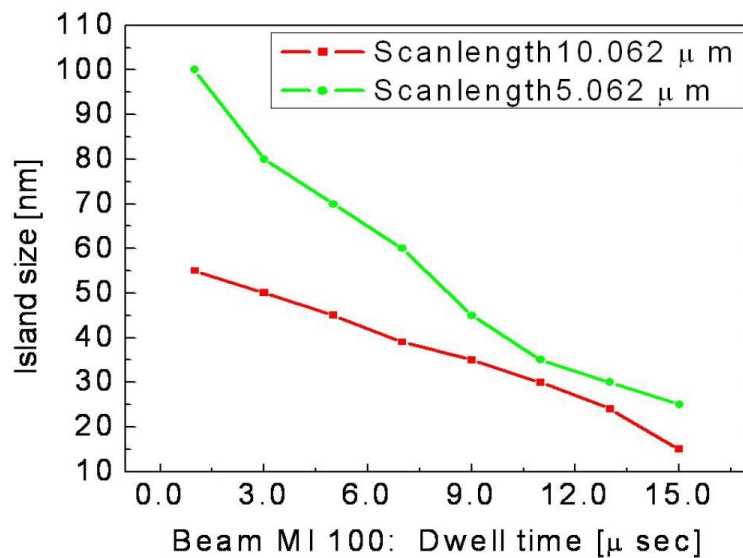


**Figure 3.20:** Control of island size with beam MI100

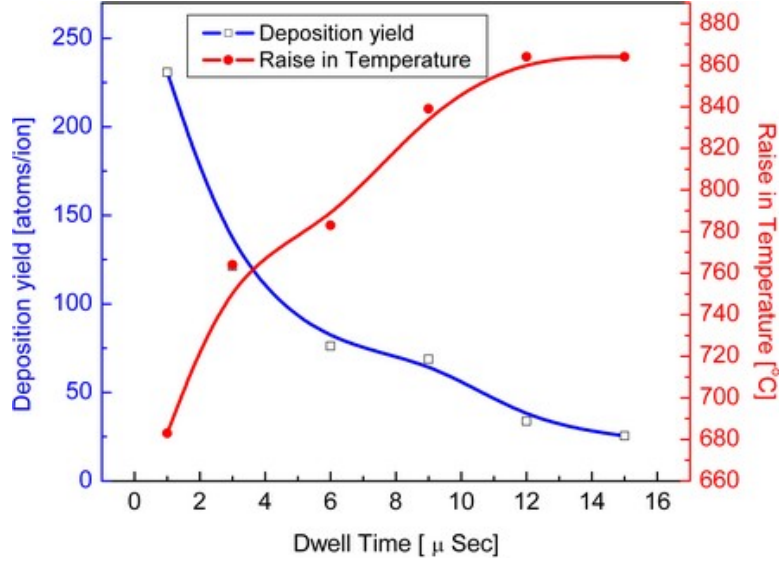
the inter pixel spacing, the amount of the material decomposed into tungsten is less, due to the inactivity of the beam at those pixels to decompose the adsorbed material into tungsten, and hence the deposition yield decreases and hence the island size. The reduction of the structure size reduces the inter pixel distance, most of the precursor material is decomposed in to tungsten increasing the deposition yield. This results in



**Figure 3.21:** Controlling island size with dwell time of beam MI-200



**Figure 3.22:** Controlling island size with dwell time of beam MI-100



**Figure 3.23:** Deposition yield and temperature raise with dwell time

increasing island size of the deposited nano particle. The beam, also, requires more dwell time to increase the sputtering effect to achieve the reduction in the deposited nano structure. The beam current is changed from 3.5nA to 0.8nA by changing the ion beam for deposition from MI 200 to beam MI 100, similar trend of reduction in the island size with the increase in the dwell time of the deposition process was observed, as shown in Figure 3.22. The effect of dwell time on the island size for different deposition structures of  $10.062\mu \times 10.062\mu\text{m}$  and  $5.062\mu\text{m} \times 5.062\mu\text{m}$  was studied and similar trend in the size of the deposited island size was confirmed with the difference in the beam current and in the dwell time of the deposited island size.

The effect of beam dwell time on the deposition yield because of the phonon generation in the sample is investigated using Finite Element Analysis. It was observed from the simulations that, the deposition yield decreased with the increase in the dwell time

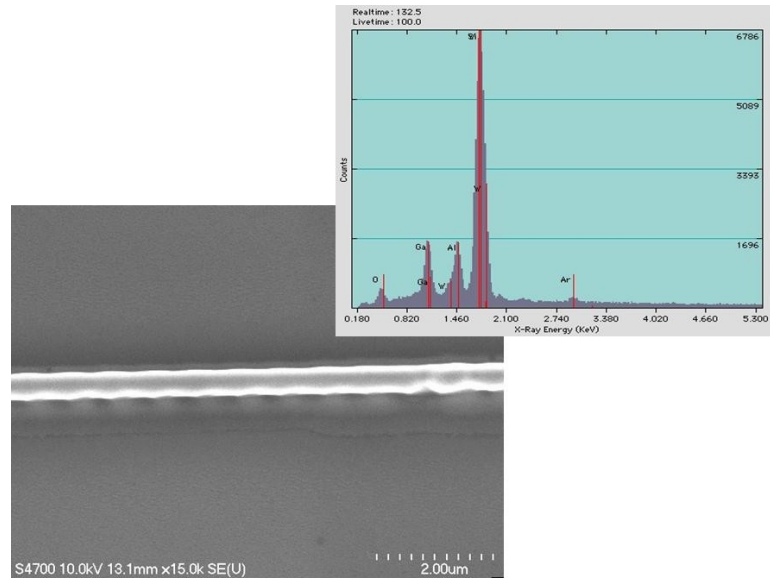
of the deposition process, as shown in Figure 3.23. The energy imparted by the ion beam to the sample is manifesting in to two different phenomenon. A part of the energy is used in the physical etching of the sample surface and more that 50 percent of the beam energy is imparted as phonon energy. It was found from the SRIM-TRIM Monte carlo simulations that, the phonon energy generated by the beam is causing an increase in the surface temperature from  $680^{\circ}\text{C}$  to  $860^{\circ}\text{C}$  with the increase in the dwell time of the process from  $1\ \mu\text{ sec}$  to  $15\ \mu\text{ sec}$ . The increase in the surface temperature is is much less than the melting point of tungsten ( $3400^{\circ}\text{C}$ ) and hence, the phonon component of the beam energy is not contributing in the ablation of the deposited tungsten thin film. It was also found that the heat energy generated in the surface thin film is conducted to the underlying layers, and hence, not contributing to the thermal ablation nor to the decomposition of  $W(CO)_6$  on the surface.

### 3.5 Chemical oxidation of Tungsten

Tungsten nano-wires 40  $\mu\text{m}$  in length and 250nm in width have been fabricated using FIB deposition. Beam 01 was used for the deposition. For the deposition of nano-wires normal deposition parameters are used. The interlace for the deposition process was set at a value 2 and the deposition time was at 4 minutes. The dimensions of the nano-wire connecting the gate was 45  $\mu\text{m}$  in length and 250 nm in width. The deposition time for the gate nano-wire was set at 5 minutes. The measuring pads for device probing were also fabricated using the beam 01 with a deposition time of 10 minutes for each measuring pad. The pad dimensions were 100  $\mu\text{m} \times 100 \mu\text{m}$ . The SEM micro graph in Figure 3.24, shows the tungsten nano-wire and the inset shows the EDS spectra of the tungsten nano-wire. The EDS results contain  $\text{Al}_2\text{O}_3$ ,  $\text{Ga}^+$ , and Si because of the underlying oxide film, the FIB  $\text{Ga}^+$  beam, and the substrate material respectively. A slight trace of Ar is also seen because of the use of the Ar plasma in sputter deposition of  $\text{Al}_2\text{O}_3$  thin film.

Tungsten nano-wires were oxidized using chemical oxidation in a solution of glacial acetic acid and hydrogen peroxide at a volume ratio of 1:1. This solution is known as peracetic acid. Peracetic acid was considered for the oxidation of tungsten because it is a strong oxidizer and was demonstrated on several refractory metal systems. The FIB fabricated nano-wires were subjected to a Piranha solution dip (sulfuric acid: hydrogen peroxide: and water in equal volumes) and a thorough rinse before

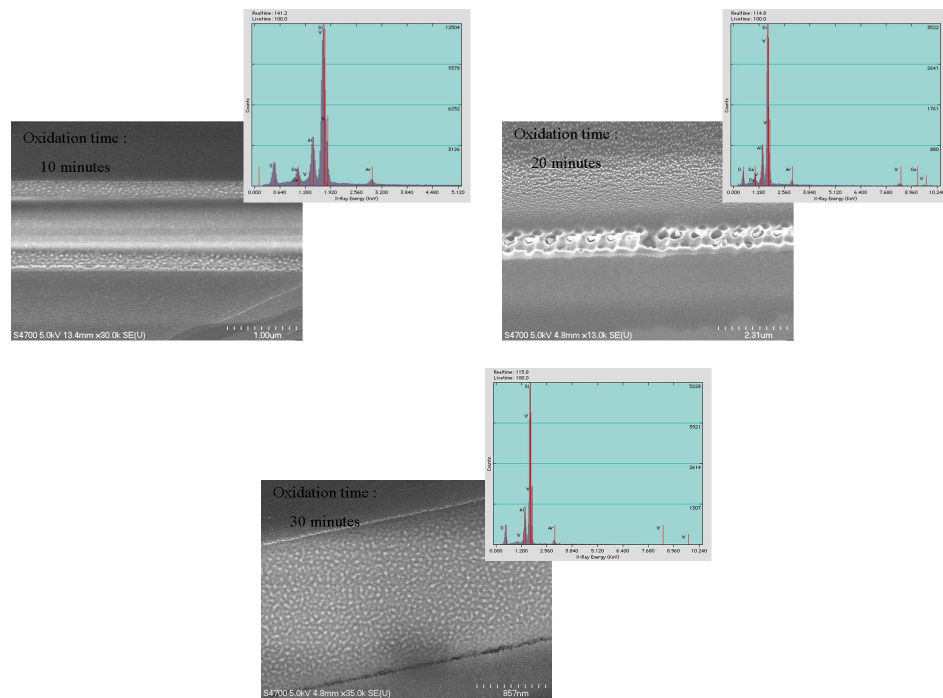




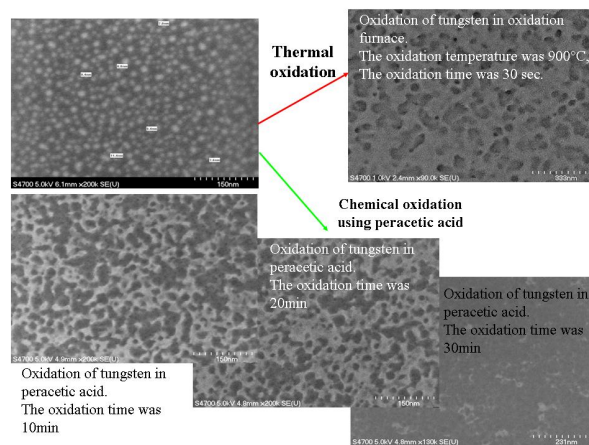
**Figure 3.24:** SEM micrograph of the tungsten nano-wire and the EDS spectra of the tungsten nano-island.

the peracetic acid oxidation. The oxidation time was varied from 10 minutes to 30 minutes. The samples were then thoroughly rinsed in de-ionized water. EDS was performed on the samples to see the change in the oxide concentration. A correlation between the oxidation time and the number of counts for the oxide was observed. Oxide growth increased up to 20 minutes and then the oxide counts decreased, showing that the oxide is dissolved in the peracetic acid after an oxidation time of 20 minutes. It can be concluded that the oxidation of tungsten dominates up to 20 minutes and the dissolution rate dominates for longer oxidation times. The SEM micro graphs and the EDS spectrum shown in Figure 3.25 confirm these results.

The initial oxidation of tungsten nano-islands was performed by thermal oxidation. It was determined that the high temperature during thermal oxidation, contributes to

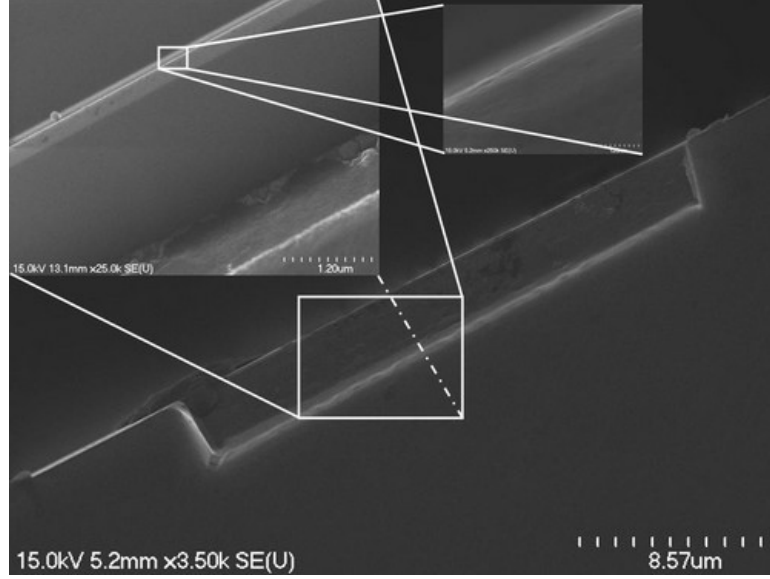


**Figure 3.25:** SEM Micrographs and the EDS micrograph of the fabricated tungsten nano-wires



**Figure 3.26:** Oxidation of tungsten nano islands.

an increase in the dimensions of the nano-structure of the quantum islands, because of the thermodynamics of the oxidation process. The increase in the island size would increase the capacitance of the island. Hence, the oxidation of tungsten nano-islands should be done at lower temperatures. The chemical oxidation method for tungsten was considered a suitable candidate for the requirement. Peracetic acid was investigated for oxidizing tungsten nano-islands. Different oxidation times, starting from 1 minute to 30 minutes were investigated. The resulting nano-structure of the oxide of tungsten was observed using SEM and EDS. The oxidation of nano-islands increased with the oxidation time and after 10 minutes of oxidation the islands were etched away because of the dissolution of the oxide in peracetic acid as shown in the Figure 3.26. The tunneling oxide for the SET device were fabricated during the oxidation process of tungsten nano-islands. The thickness of the tungsten oxide thin film is estimated from the SEM micrographs of the FIB cross sectional images of the tungsten oxide. The cross-section of the sample was polished to 1  $\mu$ m smoothness, after the sample clean, tungsten nano-islands were deposited on the edge of the smoothed surface, followed by a FIB etch removing a part of the deposited nano-islands, The SEM micrograph of the FIB etched sample surface is shown in the Figure 3.27. The Figure 3.28 shows the tungsten oxide growth on the nano-islands. It was found that the oxide thickness increases with the oxidation time, till 10 minutes and decrease thereafter because of the higher dissolution rate of tungsten in  $H_2O_2$  [70], the thickness of tungsten oxide with different oxidation times is shown



**Figure 3.27:** FIB cross sectional SEM images of tungsten oxide.

in the Figure 3.29. The thickness data is presented in the Table 3.3.

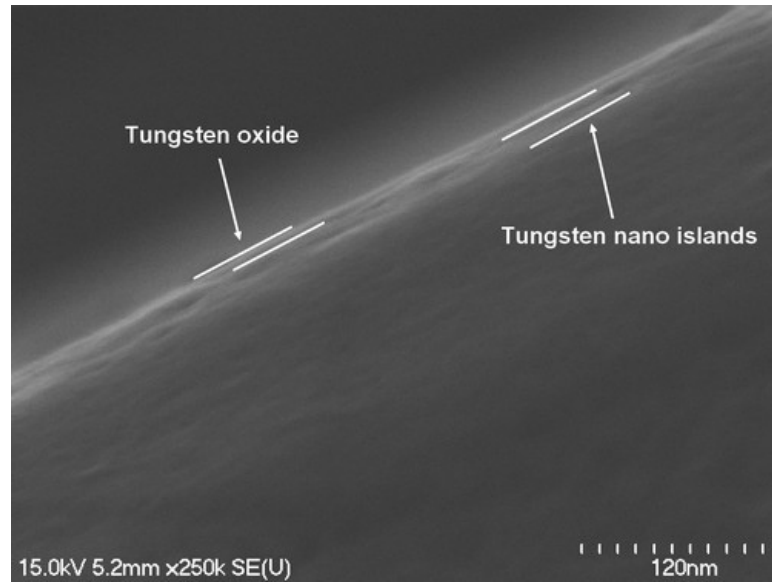
**Table 3.3:** Thickness of the tungsten oxide

Oxidation time [Minutes]	Oxide thickness [nm]
1	2.3146
2	2.8
4	3.022
6	9.59

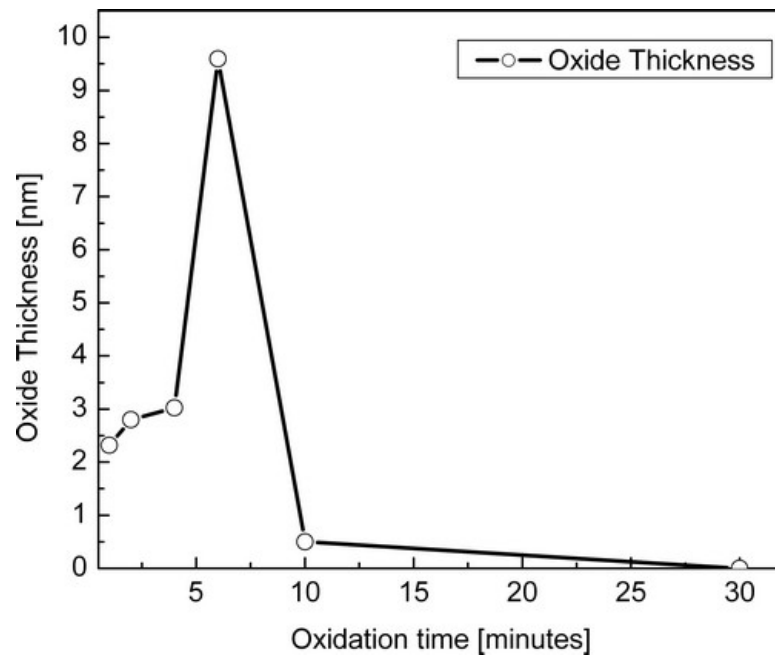
By fitting the conductance data obtained from the source-drain characteristics of the SET device to the Brinkman fit, barrier heights of the tunnel junctions were extracted.

The Brinkman fit to the conductance is given by Equ. (3.5)

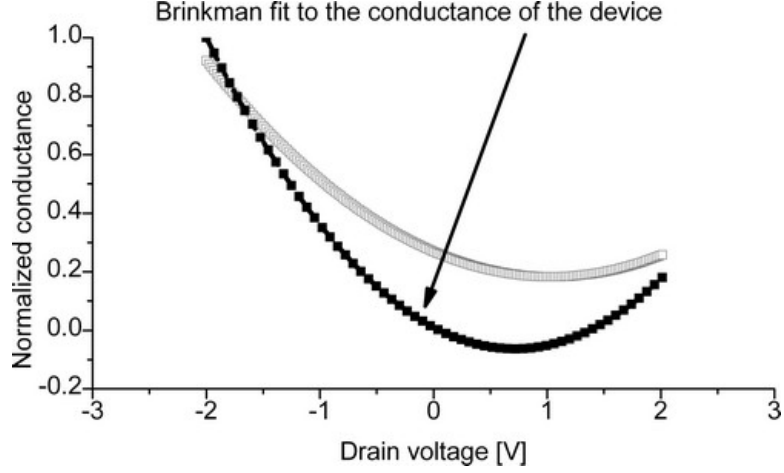
$$\frac{G(V)}{G(0)} = 1 - \left( \frac{A_0 \Delta \varphi}{16 \sqrt{[3] \bar{\varphi}}} \right) eV + \left( \frac{9 A_0^2}{128 \bar{\varphi}} \right) (eV)^2 \quad (3.5)$$



**Figure 3.28:** Thickness of the tungsten oxide.



**Figure 3.29:** Thickness of the tungsten oxide.



**Figure 3.30:** Barrier height extraction of the tunnel junction.

Where  $G(V)$  is the conductance and  $G(0) = (3.16 \times 10^{-10} \sqrt{\varphi}/d) \exp(-1.25d\sqrt{\varphi})$ , and  $\Delta\varphi = \varphi_1 - \varphi_2$ ,  $A_0 = 4(\sqrt{2m}) \frac{d}{3\hbar}$ . The voltage at which the conductance minimum occurs is related to other parameters of the junction as  $eV_{min} = 0.649(\frac{\Delta\varphi}{d\sqrt{\varphi}})$ , by knowing the voltage at which the conductance minimum occurs, and the linear and quadratic pre factors of the Brinkman fit, the effective barrier height of the tunnel junction could be extracted [71]. The Brinkman fit to the experimental data is presented in the Figure 3.30. The conductance fit to the tunnel barriers varying in thickness were investigated to obtain the barrier height for different thickness of the tunnel junction. The barrier heights extracted using the Brinkman fit method are found to be 2.33 eV, 1.865 eV, and 1.367 eV respectively for 2.214 nm, 3.022 nm and 9.59 nm thin films.

## 3.6 Process Integration for the SET

Fabrication of SET devices requires the fabrication of individual elements of the device; which are the conducting nano-particles, the tunnel junctions the nano-scaled leads connecting the active area of the device to the micro scaled probing pads. The integration of the process of these individual elements of the device result in two main categories of device fabrication. Depending on the sequence of nano-island fabrication in the process flow, the fabrication sequence can be classified in to two different categories:

1. Pre island fabrication process.
2. Post island fabrication process.

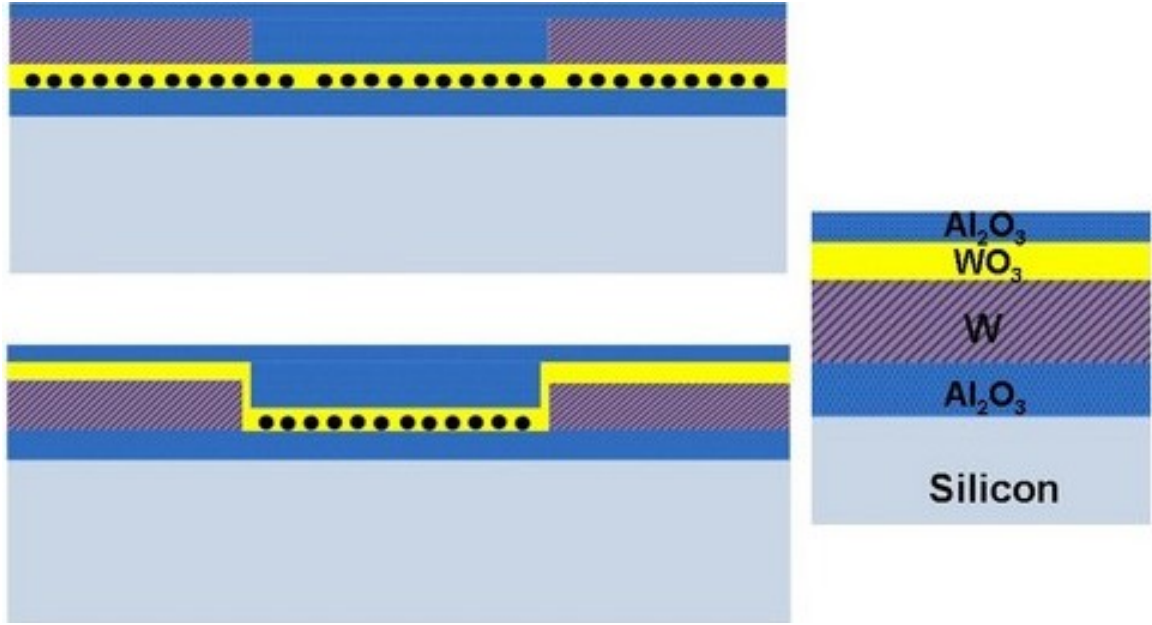
In the Pre island fabrication process, the nano and micro scaled structures are fabricated after the nano-particle fabrication, where as in the post island fabrication process the nano-particles are fabricated after the fabrication of the nano and micro scaled structures.

The process flow for the fabrication of SETs using these different methods is presented in the Figure 3.31. The fabrication of SET starts with the bare silicon wafer. The silicon wafer is thoroughly cleaned in piranah solution, followed by a through rinse in DI water, and dried in nitrogen ambient. Following the sample clean, 300nm thick  $Al_2O_3$  film is deposited on the silicon wafer, using 2400-8J Perkin Elmer parallel

plate RF sputtering system. The  $Al_2O_3$  layer acts as an isolation layer. After the deposition of isolation layer, the sample is introduced in to the Hitachi FB-2000A focused ion beam system to fabricate the conducting nano islands of tungsten(detailed procedure of fabrication is given in Appendix). After the nano-island fabrication the sample is introduced in to the peracetic acid to form tungsten oxide, which acts as the tunneling junctions. Then the sample is reintroduced in to the Hitachi FIB system to fabricate the nano-scaled leads which connect the active device area to the micro scaled probing pads, which are also fabricated using FIB deposition. These nano-scaled connecting leads and the micro scaled probing pads can also be fabricated using lithographic techniques capable of fabrication sub micron structures. Nanoimprint lithography is one such available technique to fabricate these structures. Following the fabrication of nano scaled and micro scaled structures, a 30 nm thin film of  $Al_2O_3$  is sputtered on the device. The  $Al_2O_3$  thin film acts as a passivating layer for the device. The probing pads of the device are etched away using FIB etching to expose the source, drain and gate terminals of the device.

The SET devices with nano-island first and nano-island last process have been fabricated. SET devices having different thickness of the tunneling oxide have been fabricated to investigate the effect of the thickness on the device characteristics. SET device which have different geometries of the electrodes in the active area of the device have been fabricated. The different devices with different device topologies are explained in the next section.



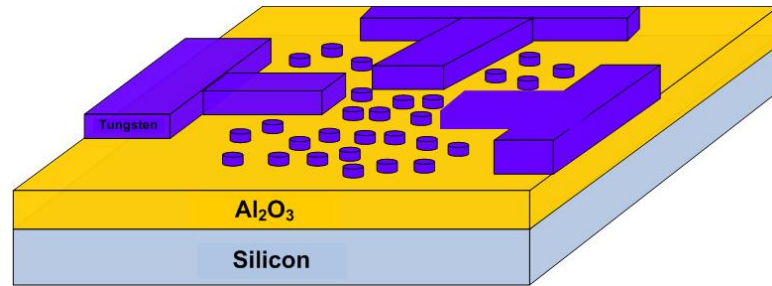


**Figure 3.31:** Process flow for the fabrication of SET using FIB deposition

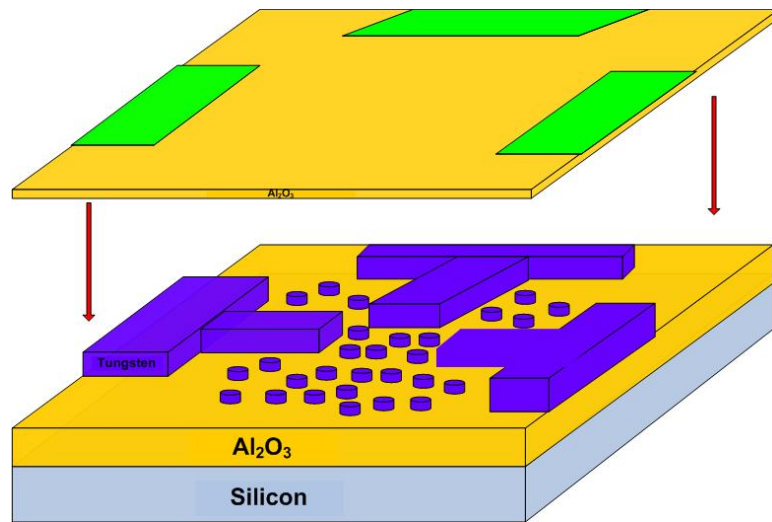
### 3.7 Device topologies for the SET

In the fabrication of the nano islands the two possible schemes of device fabrication are explored to see the difference in the device characteristics of an SET. The two different schemes are pre island deposition scheme and a post island deposition scheme. In the Pre island deposition scheme the measuring pads for the device are fabricated after the formation of the oxide which acts as the tunneling barrier, where as in the post island deposition scheme the nano-island and the measuring pads are fabricated in the same processing step, then a layer of thin oxide is created using peracetic acid oxidation to form the tunneling barrier. The schematic in Figure 3.32 shows the cross section device after fabrication.

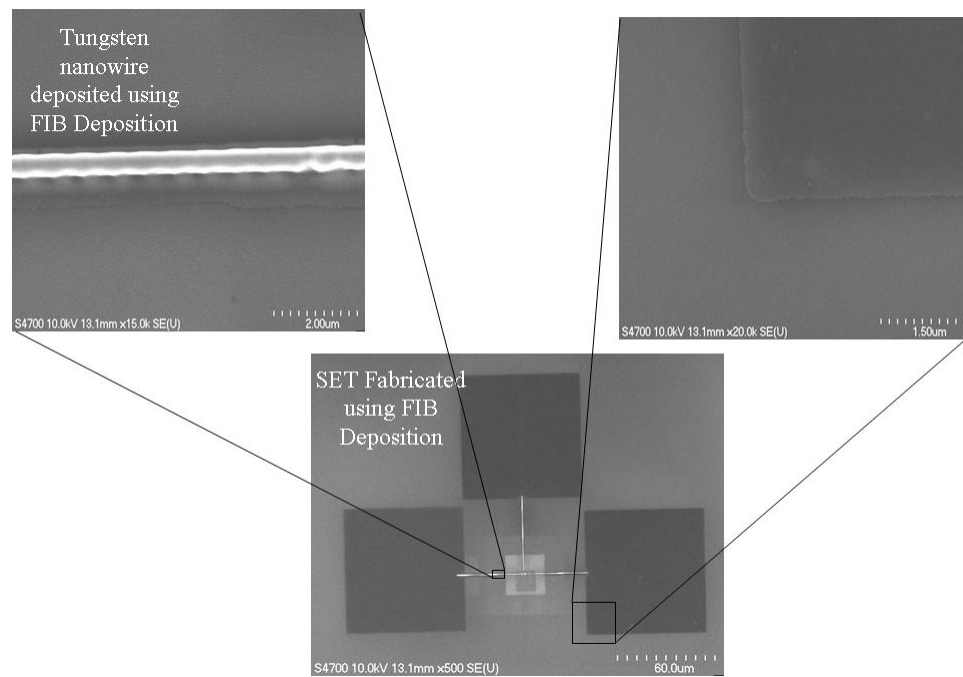
SET devices having QD-first and QD-last processes have been fabricated. Both fabrication sequences have been used to demonstrate devices with different electrode terminations near the quantum dot active area. These different device structures differ in the way the electric field is applied on the quantum islands. The electric field in the vicinity of the quantum islands is different, and this also impacts the total capacitance of the device. Hence different device characteristics are expected for these devices. The fabricated SET structures have different device fabrication scheme and with in each device fabrication scheme, the electrode placement is different. The difference in the electrode placements results in different device topologies. For each device topology there are three different termination configurations for the devices, also having different tungsten oxide thickness. The different devices have three different oxidation times 2minutes, 4 minutes and 6 minutes. A blanket oxide of  $Al_2O_3$  is sputtered on the devices to eliminate any ambient environmental effects on the device characteristics as shown in Figure 3.33. The measuring pads for the device are opened up using FIB etching. The SEM micrographs of the fabricated SET structures are shown below in Figure 3.34.



**Figure 3.32:** Pictorial view of the cross section of the fabrication of SET using FIB deposition



**Figure 3.33:** Pictorial view of the cross section of the fabrication of SET with passivating oxide using FIB deposition

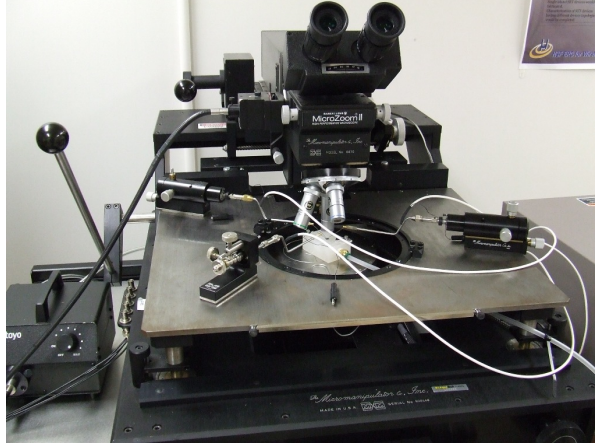


**Figure 3.34:** SEM micrograph of the fabricated SET device.

# Chapter 4

## Results

The device characteristics of the fabricated SET devices using FIB technologies are presented in this chapter. The measurement setup for the device characterization is explained in the section 4.1. Following the experimental setup, the device characteristics of the FIB etching based devices are presented in section 4.2. The results for the devices fabricated using FIB deposition are presented in section 4.3. The section on the FIB deposition based SET devices include the device characteristics for different device configurations.



**Figure 4.1:** Experimental setup for the device probing.

## 4.1 Experimental setup for SET device probing

The SET devices fabricated using FIB technologies have been characterized using the Keithley 4200 SCS semiconductor parametric analyzer system, in conjunction with the micromanipulator probing station. The experimental setup for the device probing is shown in the Figure 4.1.

The individual micromanipulator probes are connected to the source measure unit (SMU) of the 4200 SCS system. The manipulator probes are arranged on to the probing pads of the SET device using an optical microscope on the micromanipulator probing station. After the arrangement of the probes, the Keithley 4200 SCS instrument is set up to measure the device characteristics of the SET (detailed explanation on the probing of the SET device is presented in the Appendix section). The important device characteristics of the SET, which show the single electron effects are the

coulomb blockade and the coulomb oscillations. The coulomb blockade characteristics of the device represent the variation in the drain current with the variation in the source-drain voltage for a given gate bias, whereas, the coulomb oscillations of the SET device represent the variation in the drain current with the variation in the gate voltage, for a fixed source-drain voltage.

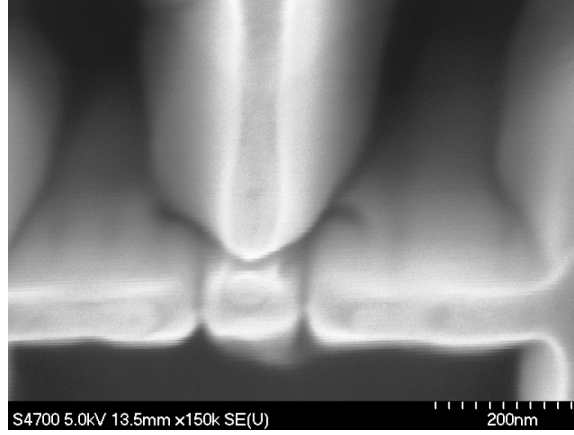
To probe the coulomb blockade behavior of the SET device, A voltage sweep on the source-drain terminals is applied. The applied voltage is varied from negative to positive voltage with a fixed incremental voltage. The incremental voltage can be decided by the 4200 SCS system, which determines the number of data points collected. The probe on the gate terminal is arranged to have a voltage step starting at a particular voltage and stopping at a different voltage, again the step interval can be decided by the 4200 SCS system. The coulomb blockade characteristics of the SET are obtained for a fixed gate voltage, by plotting the drain current against the source drain sweep voltage. The coulomb blockade characteristics are repeated for different gate voltages. The characteristics of the coulomb blockade are that, when the electrostatics of the system are not favorable for electron transfer, there is no increase in the drain current for an increase in the source-drain voltage, this is referred as coulomb blockade. For a fixed Source-drain voltage, the coulomb blockade is lifted and then the drain current increase, until the voltage reaches the next blockade event. The regions where there is no increase in current are called as the coulomb blockade events. The coulomb oscillations are obtained by sweeping the gate voltage, for a

fixed source drain voltage. The drain current shown, the coulomb oscillations with the variation in the gate voltage. The drain current is plotted against the gate voltage to obtain the coulomb oscillations, for different source-drain voltages.

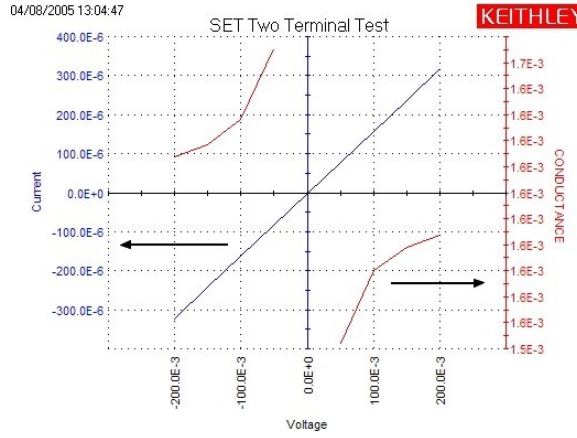


## 4.2 FIB Etching based devices

SET devices fabricated using FIB etching are fabricated on a lithographically patterned Nickel thin film. The device fabrication includes, the fabrication of tunnel junctions, the probing pads by the FIB etching. The conducting island is also fabricated as a part of the FIB etching process. Different SET devices varying in the tunnel junction width and varying in the island dimensions have been characterized for the room temperature operation [55]. The SEM micrograph of the fabricated device is shown in Figure 4.2. The source drain characteristics of the fabricated SET at room temperature are shown in Figure 4.3, the graph also shows the conductance of the device, with the variation in the source-drain voltage. The source-drain characteristics of the device with 20nm tunnel junction were obtained from -200.0 mV to 200.0 mV. The drain current resulting due to the variation in the source-drain voltage is plotted, along with the conductance of the device. For the device with 30nm tunnel junctions, as shown in the SEM micrograph of Figure 4.4, the device characteristics were obtained from -800.0 mV to 800.0 mV. The drain current and the conductance are shown in Figure 4.5. It can be seen that the drain current is linear with the range of few milli-Amps. The linearity in the device characteristics confirms the resistive behavior, hence, coulomb blockade is not observed at room temperature for these devices. The slope of the characteristics is different for both the devices, because of the differences in the island size and the tunnel junction widths. The variation in



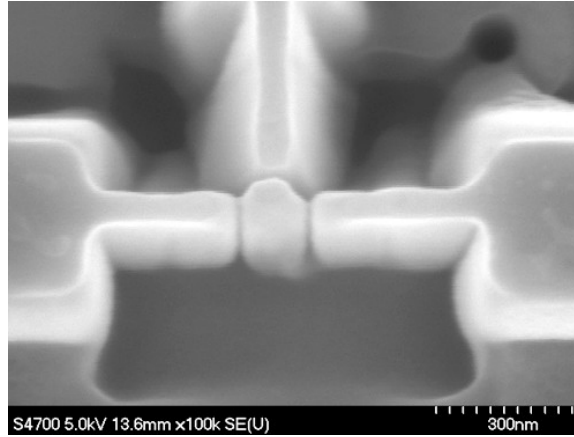
**Figure 4.2:** SEM micrograph of a 20 nm tunnel junction device.



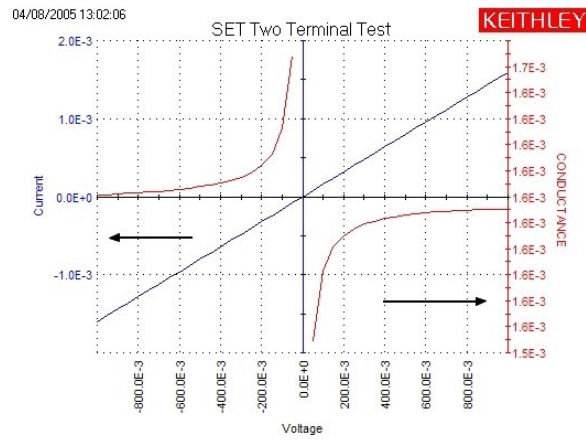
**Figure 4.3:** Output conductance the SET device at room temperature for a fixed Gate voltage.

the device parameters are a result of the variation in the fabrication process of these devices.

The conclusions from the FIB etching based devices is that the minimum conducting island size that can be fabricated, is 40nm, and the device characteristics obtained for such a device are not showing the coulomb blockade characteristics at room temperature. Hence different alternatives for the fabrication of sub 10nm conducting islands



**Figure 4.4:** SEM micrograph of a 30 nm tunnel junction device.



**Figure 4.5:** Output conductance of the SET device at room temperature for a fixed Gate voltage.

should be explored for the fabrication of room temperature operating SET devices.

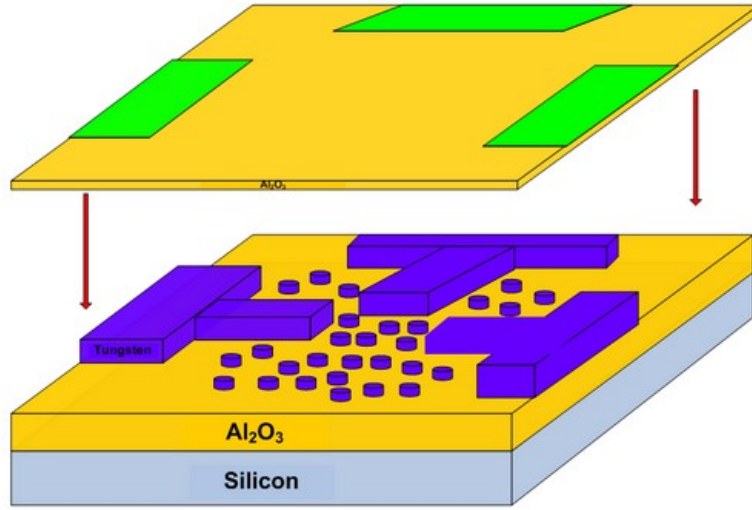
### 4.3 Room temperature operation of SET-FIB Deposition based devices

The SET devices fabricated using FIB deposition technology, show the room temperature operation. The reduction in the device capacitance, due to the decrease in the island size is a crucial factor contributing towards the room temperature operation of the device. The capacitance of the device is determined by the geometry of the conducting nano-islands and the geometry of the nano-structures in the vicinity of the conducting islands. To understand the effects of the geometry of the nano electrodes on the device characteristics, different device configurations of the nano-electrodes in the active area of the SET device were investigated. The modulation of the device characteristics with the variation in the tunnel junction thickness were also investigated. Based on the deposition of nano- particles, the devices were divided in to two different categories: The pre-island fabricated devices and the post-island fabricated devices. In each section device results for the above two configurations are presented. Device configurations differ in the active area of the device, and hence affect the transport of electrons in the device, resulting in variation of device characteristics and device parameters.

### 4.3.1 Device configuration DT1

The fabrication process for different devices remains the same except, for, the final step of active device fabrication. Different device configurations have different active electrode configurations. The device configuration where the source, drain or gate terminals do not have any extrusions is called as device configuration DT1. The active area of the device DT1 is shown in Figure 4.6. The source and drain terminals are 250 nm wide and are separated by 250nm, from each other. Based on the nano-island size ( 8nm)and the inter island spacing( 4nm), it is estimated that there are ten nano-islands, present between source and drain terminals. Hence it can be concluded that the device is made up of ten nano-islands, hence a multi dot system, where, all the ten nano-islands participate in the conduction process. From the SEM micrograph of the fabricated SET device, shown in Figure 4.7, it can be seen that there are two dimensional matrix of nano-islands present between the source and drain terminals. The electrostatics of the system make it possible for only one array to participate in the conduction process.

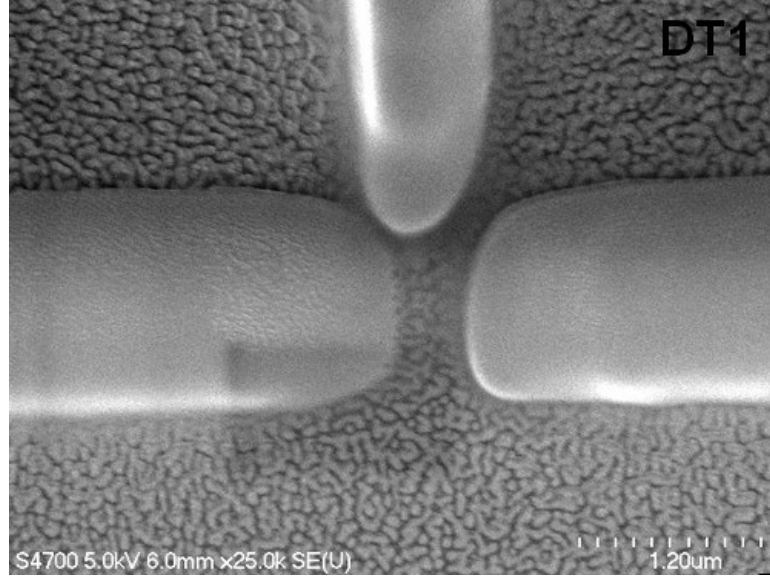
The non linear device characteristics for the device configuration DT1, fabricated using the pre-island fabrication method are shown in the Figure 4.8. The source-drain voltage is swept from -5.0 V to +5.0 V. It can be seen that the drain current is in the range of few tens of pA. The coulomb blockade characteristics for different gate voltages of -90.0 mV , -50.0 mV and -10.0 mV are shown. The device characteristics



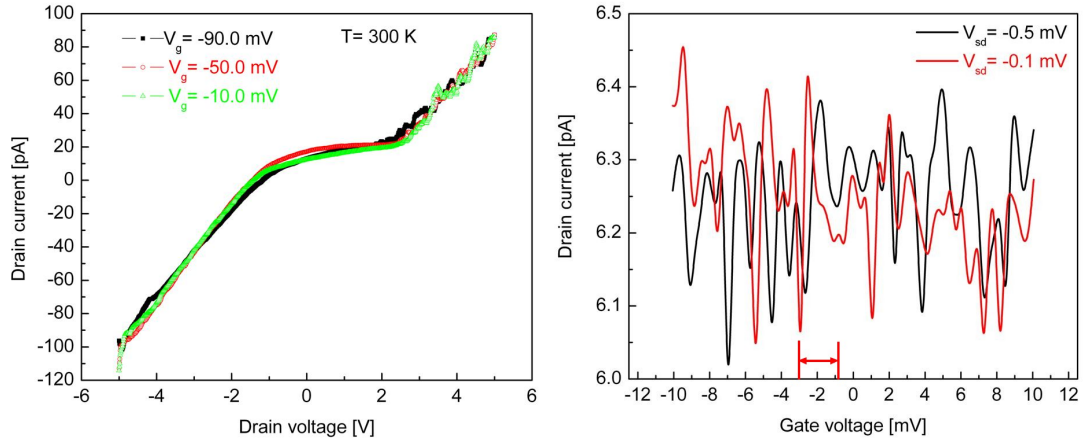
**Figure 4.6:** Pictorial view of the Device configuration DT1.

show a clear coulomb blockade characteristics. The blockade voltage obtained from the characteristics is 3.5 V. Clear coulomb oscillations in drain current are observed with the variation in the gate voltage, shown the charging and discharging of the conducting nano islands, The period of the coulomb oscillations was found to be 2.2 mV.

The Coulomb oscillations in the drain current, for a fixed source-drain voltage are clearly observed with the change in the gate voltage. The clear oscillations in the drain current represent the charging and discharging of the quantized states in the conducting nano-islands, resulting from the coulomb blockade effect. The Coulomb oscillations for a single dot SET system are periodic, but for a multi dot SET system because of the non-uniformity in size of the nano-islands, and also the non-uniformity

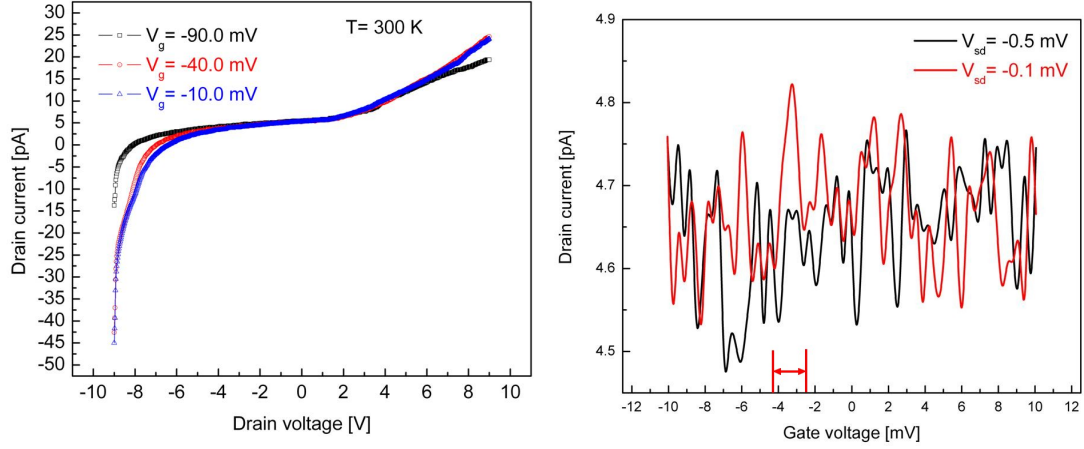


**Figure 4.7:** SEM micro graph of the Device configuration DT1.



**Figure 4.8:** Coulomb blockade and coulomb oscillations of the SET device configuration DT1 Pre fabricated island

in the island spacing, the Coulomb oscillations are aperiodic in nature [72]. The gate voltage is varied from -12.0 mV to 12.0 mV, for fixed source-drain voltages of -0.1 mV and -0.5 mV. It can be seen that the drain current oscillates with the change in the



**Figure 4.9:** Coulomb blockade and coulomb oscillations of the SET device configuration DT1 Post fabricated island

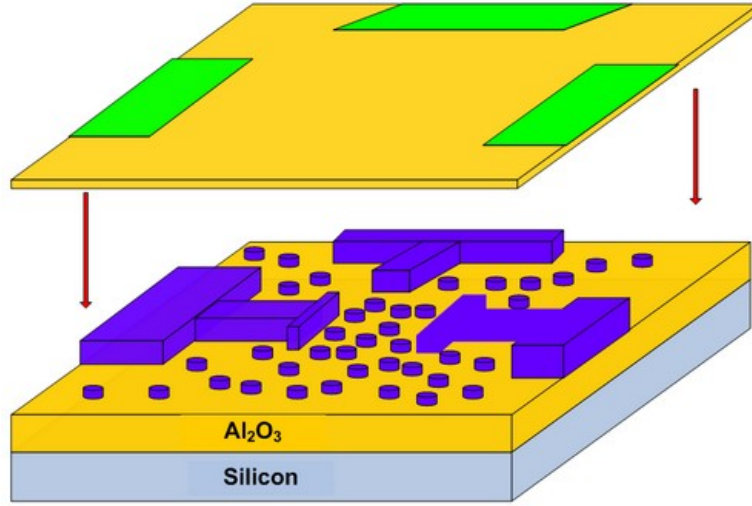
gate voltage.

The non linear device characteristics of the device configuration DT1, fabricated using the post-island fabrication method are shown in the Figure 4.9, the source-drain voltage is swept from -10.0 V to +10.0 V. It can be seen that the drain current is in the range of few tens of pA. The coulomb blockade characteristics for different gate voltages of -90.0 mV , -5-.0 mV and -10.0 mV are shown. The device characteristics show a clear coulomb blockade characteristics. The coulomb blockade voltage obtained from the characteristics is 8.5 V.

The coulomb oscillations in the drain current, for a fixed source-drain voltage are clearly observed with the change in the gate voltage. The clear oscillations in the drain current represent the charging and discharging of the conducting nano islands, resulting from the coulomb blockade effect. The gate voltage is varied from -12.0 mV



to 12.0 mV, for fixed source-drain voltages of -0.1 mV and -0.5 mV. It can be seen that the drain current oscillates with the change in the gate voltage, having an average period of 3.0 mV.

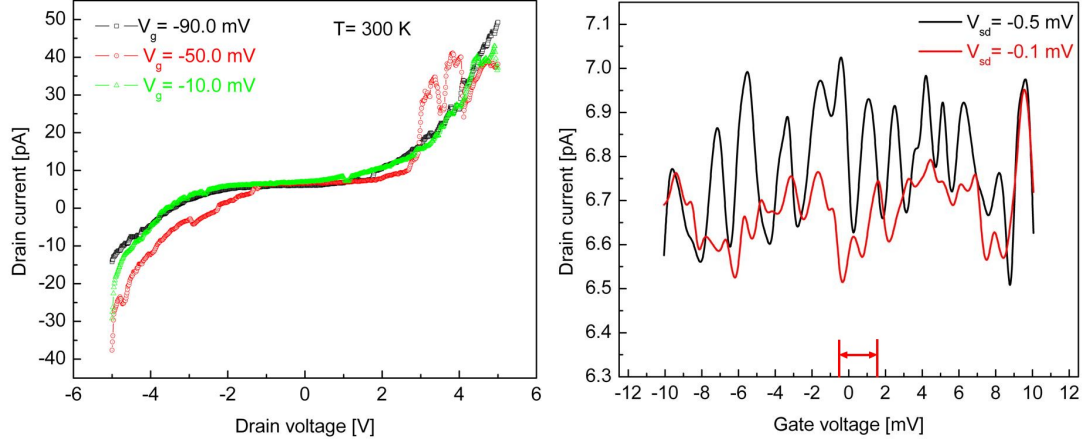


**Figure 4.10:** Pictorial view of the Device configuration DT2.

### 4.3.2 Device configuration DT2

The device configuration where the source, drain terminals do not have any extrusions, and the gate terminal have an extrusion is called as device configuration DT2. The active area of the device DT2 is shown in Figure 4.10. The source and drain terminals are separated by 250nm, and have the width of 250nm, based on the nano island size ( 8nm)and the inter island spacing( 4nm), it is estimated that there are ten nano islands participating in the conduction process. The gate terminal of the device is closer to the source drain terminals compared to the configuration DT1. The proximity of the gate terminal to the source drain terminals will change the geometric arrangement of the nano leads, and also change the over all capacitance of the device.

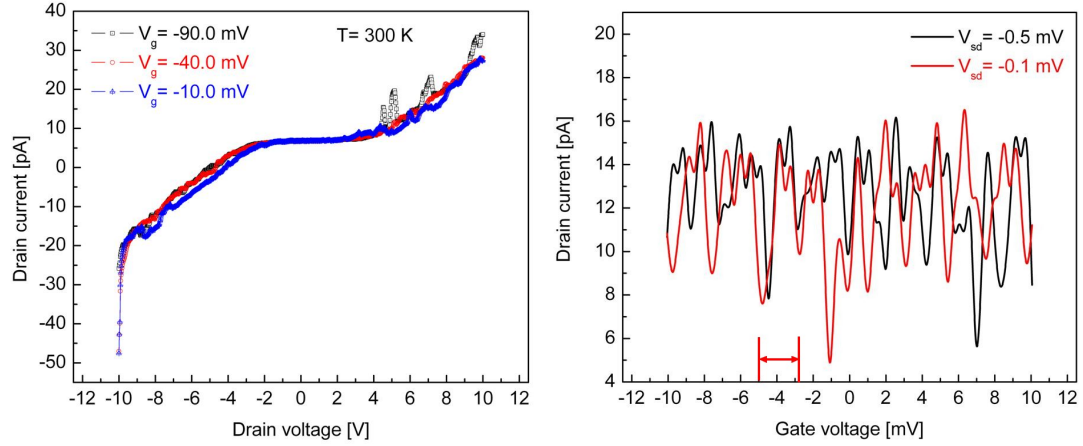
The non linear device characteristics of the device configuration DT2, fabricated



**Figure 4.11:** Coulomb blockade and coulomb oscillations of the SET device configuration DT2 Pre fabricated island

using the pre-island fabrication method are shown in Fig 4.11. The drain current as a function of source-drain voltage is shown in the Fig 4.11, the source-drain voltage is swept from -5.0 V to +5.0 V. It can be seen that the drain current is in the range of few tens of pA. The coulomb blockade characteristics for different gate voltages of -90.0 mV , -50.0 mV and -10.0 mV are also shown. The device characteristics show a clear coulomb blockade characteristics. The coulomb blockade voltage obtained from the characteristics is 5.0 V.

The coulomb oscillations in the drain current, for a fixed source-drain voltage are clearly observed with the change in the gate voltage. The clear oscillations in the drain current represent the charging and discharging of the quantized charge states in the nano-island, resulting from the coulomb blockade effect. The aperiodic Coulomb oscillations are attributed to the non-uniformity in island size and spacing of the nano-islands. The gate voltage is varied from -12.0 mV to 12.0 mV, for fixed source-



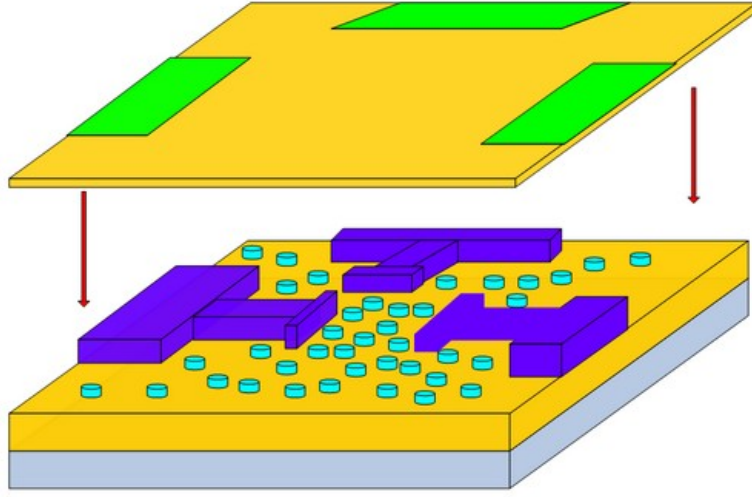
**Figure 4.12:** Coulomb blockade and coulomb oscillations of the SET device configuration DT2 Post fabricated island

drain voltages of -0.1 mV and -0.5 mV. It can be seen that the drain current oscillates with the change in the gate voltage, the average period of coulomb oscillation was found to be 3.0 mV.

The non linear device characteristics of the device configuration DT2, fabricated using the post-island fabrication method are shown in the Figure 4.12, the source-drain voltage is swept from -10.0 V to +10.0 V. It can be seen that the drain current is in the range of few tens of pA. The coulomb blockade characteristics for different gate voltages of -90.0 mV , -50.0 mV and -10.0 mV are shown. The device characteristics show a clear coulomb blockade characteristics. The coulomb blockade voltage obtained from the characteristics is 7.0 V.

The coulomb oscillations in the drain current, for a fixed source-drain voltage are clearly observed with the change in the gate voltage. The clear oscillations in the

drain current represent the charging and discharging of the conducting nano islands, resulting from the coulomb blockade effect. The gate voltage is varied from -12.0 mV to 12.0 mV, for fixed source-drain voltages of -0.1 mV and -0.5 mV. It can be seen that the drain current oscillates with the change in the gate voltage, showing the charging and discharging of the conducting islands. The average period of the coulomb oscillations was found to be 2.1 mV.

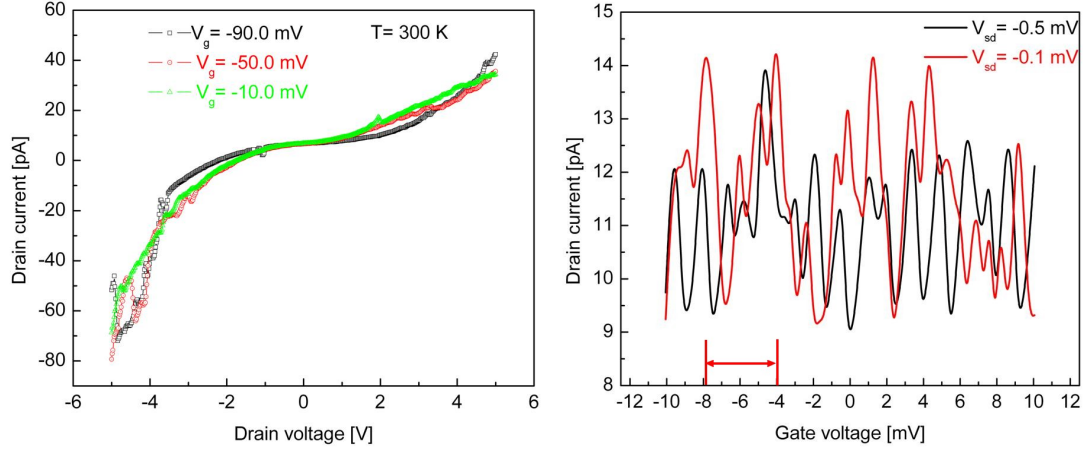


**Figure 4.13:** Pictorial view of the Device configuration DT3.

### 4.3.3 Device configuration DT3

The device configuration where the source, drain and gate terminals have an extruding structure is called as device configuration DT3. The active area of the device DT3 is shown in Figure 4.13. The source and drain terminals are separated by 250nm, and have the width of 250nm, based on the nano-island size ( 8nm)and the inter island spacing( 4nm), it is estimated that there are ten nano islands participating in the conduction process. The proximity of the gate terminal to the source drain terminals, and the extrusions on the source drain terminals will change the geometric arrangement of the nano leads, and also change the over all capacitance of the device.

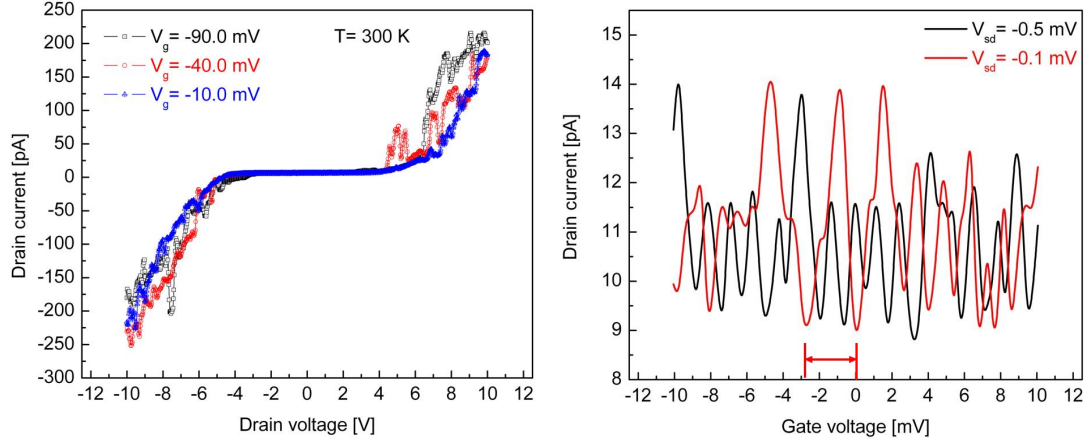
The non linear device characteristics of the device configuration DT3, fabricated using the pre-island fabrication method are shown in the Figure 4.14, the source-drain



**Figure 4.14:** Coulomb blockade and coulomb oscillations of the SET device configuration DT3 Pre fabricated island

voltage is swept from -5.0 V to +5.0 V. It can be seen that the drain current is in the range of few tens of pA. The coulomb blockade characteristics for different gate voltages of -90.0 mV , -50.0 mV and -10.0 mV are shown. The device characteristics show a clear coulomb blockade characteristics. The coulomb blockade voltage obtained from the characteristics is 2.0 V.

The coulomb oscillations in the drain current, for a fixed source-drain voltage are clearly observed with the change in the gate voltage. The clear oscillations in the drain current represent the charging and discharging of the quantized charge states in the nano-island, resulting from the coulomb blockade effect. The aperiodic Coulomb oscillations are attributed to the non-uniformity in island size and spacing of the nano-islands. The gate voltage is varied from -12.0 mV to 12.0 mV, for fixed source-drain voltages of -0.1 mV and -0.5 mV. It can be seen that the drain current oscillates with the change in the gate voltage, the period os coulomb oscillations was found to



**Figure 4.15:** Coulomb blockade and coulomb oscillations of the SET device configuration DT3 Post fabricated island

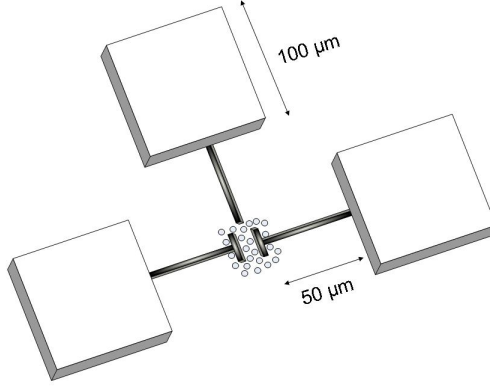
be 4.0 mV.

The non-linear device characteristics of the device configuration DT3, fabricated using the post-island fabrication method are shown in the Figure 4.15, the source-drain voltage is swept from -10.0 V to +10.0 V. It can be seen that the drain current is in the range of few tens of pA. The coulomb blockade characteristics for different gate voltages of -90.0 mV , -5-.0 mV and -10.0 mV are shown. The device characteristics show a clear coulomb blockade characteristics. The coulomb blockade voltage obtained from the characteristics is 8.0 V.

The coulomb oscillations in the drain current, for a fixed source-drain voltage are clearly observed with the change in the gate voltage. The clear oscillations in the drain current represent the charging and discharging of the conducting nano islands, resulting from the coulomb blockade effect. The gate voltage is varied from -12.0 mV



to 12.0 mV, for fixed source-drain voltages of -0.1 mV and -0.5 mV. It can be seen that the drain current oscillates with the change in the gate voltage, the period of coulomb oscillations was found to be 3.0 mV.

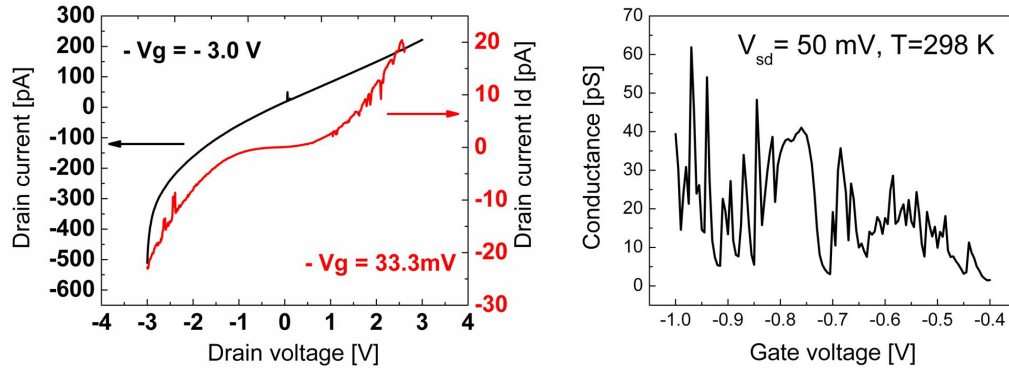


**Figure 4.16:** Pictorial view of the Device configuration DT4.

#### 4.3.4 Device configuration DT4

The pictorial view of the device configuration DT4 is shown in Fig 4.16, where the source and drain terminals have the extra electrode. The room temperature current-voltage ( $I$ - $V$ ) characteristics of the device with the source-drain voltage ( $V_{sd}$ ) swept from -3.0 V to +3.0 V at the gate bias ( $V_g$ ) of -3.0 V and 33.3 mV is shown in Fig 4.17. It can be seen from the non-linear  $I_d$ - $V_{sd}$  characteristics of the device in Figure 4.16 that the Coulomb blockade is clearly visible for the gate voltage bias of 33.3 mV. For a higher gate voltage of -3.0 V, the Coulomb blockade is not prominent. The drain current of the device is on the order of pA, and the magnitude of the drain current changes by two orders of magnitude for a change of 3.3 V in gate bias.

Figure 4.17 shows the Coulomb oscillations in the device with respect to the gate voltage  $V_g$ . The  $V_g$  was swept from -1.0 V to -0.8 V for a fixed  $V_{sd}$  of 50.0 mV [56].



**Figure 4.17:** Coulomb blockade and coulomb oscillations of the SET device DT4

The Coulomb oscillations are visible for the applied source-drain voltage. The drain current, which is in the pA range, oscillates periodically with the increase in the gate bias, showing clearly that the oscillations arise from the confinement of electrons on the tungsten quantum islands.

# Chapter 5

## Analysis and Discussion

### 5.1 FIB Etching based devices

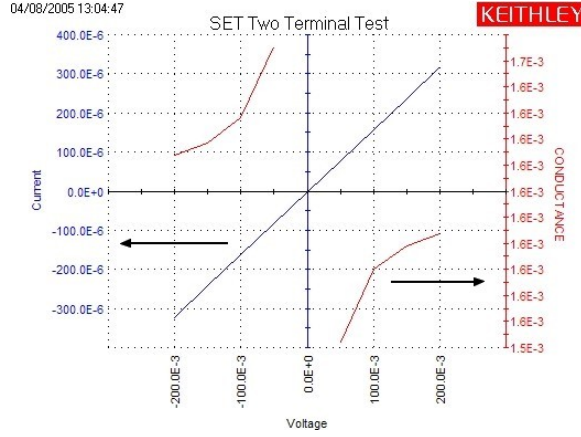
The source drain characteristics of the fabricated SET at room temperature are shown in Figure 5.1 and Figure 5.2. The tunnel resistance of the SET was calculated from the I-V characteristics. These calculations indicate that the SET is operating in the strong tunneling regime, with a tunnel resistance comparable in magnitude to the quantum resistance. The tunnel resistance of the device with a 20nm tunnel junction width has a tunnel resistance of  $5k\Omega$  and the device with tunnel junction width of 30nm has a tunnel resistance of  $22k\Omega$ . The tunnel resistance being comparable to the quantum of resistance results in a broadening and overlap of excited charge states, thus causing suppression of the single charge effects due to charge dissipation [73].

The amplitude of the oscillations decay exponentially at higher temperatures [74] demonstrating linear device characteristics. For the present case of strong tunneling at higher temperatures, the observed conductance reaches its asymptotic value as shown in Figure 5.1 and Figure 5.2. The device with the tunneling gap of 20nm had a tunnel resistance of  $5k\Omega$ . Hence, the conductance of the device is more than the conductance of the device with 30nm tunnel junction width and the tunnel resistance of  $22k\Omega$ . The differences in the island size also contribute to the difference in conductances, but the tunnel resistance of the device is a dominant factor affecting the conductance of the device. Hence, by varying the width of the tunnel junction in the fabrication process the tunnel resistance of the SET can be controlled in the FIB etching process.

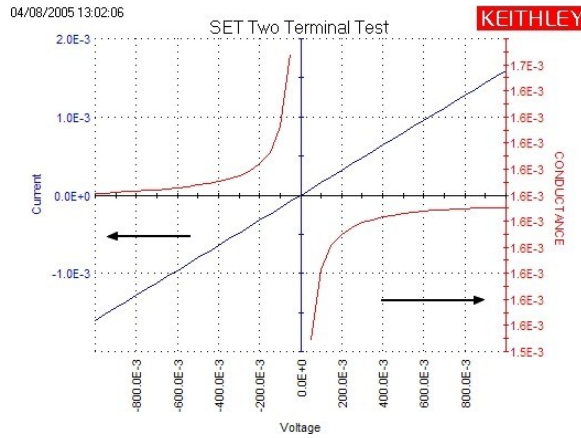
The combined resistance of the device was calculated from the I-V characteristics of the device and the device with the tunneling gap of 20nm had a tunnel resistance of  $5k\Omega$  and the device with 30nm tunnel junction width had the tunnel resistance of  $22k\Omega$ . because of the difference in the tunnel resistance and the difference in the charging energies of the devices the conductance of the devices vary from each other.

$$G_T = \frac{1}{R_\Sigma} \left( 1 - \frac{E_C}{3T} + \dots \right) \quad (5.1)$$

The conductance of the device is calculated for different tunnel resistances of the device. The conductance of the SET device in the strong tunneling regime is given by the Equ. (5.1), and it depends on the tunnel resistance, and the charging energy of the



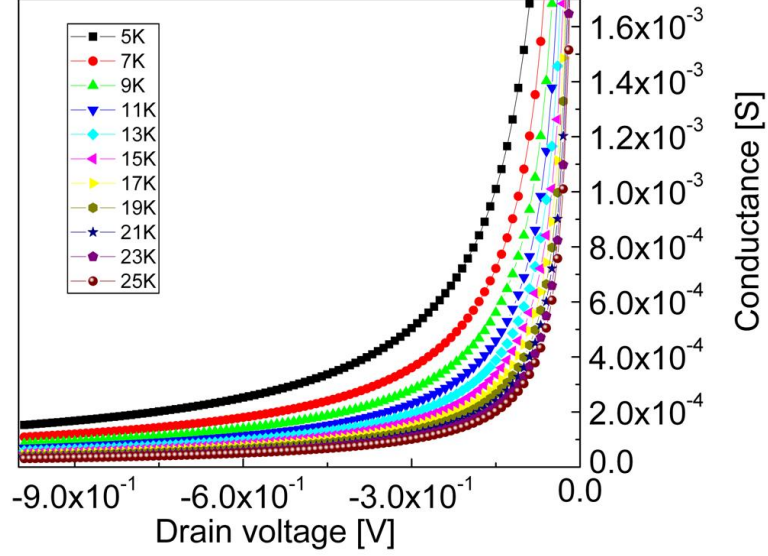
**Figure 5.1:** Output conductance the SET device at room temperature for a fixed Gate voltage.



**Figure 5.2:** Output conductance of the SET device at room temperature for a fixed Gate voltage.

device. The conductance of the device for different tunnel resistance varying from  $5k\Omega$  to  $25k\Omega$  is calculated as shown in Figure 5.3. It is seen that for lower tunnel resistance junctions the conductance is higher and vice-versa. The experimental observation in the variation in the conductance is verified by the theoretical calculation of the conductance.

SET devices with different tunnel widths and different island sizes were fabricated



**Figure 5.3:** Theoretical calculations of the SET conductance with drain voltage.

using FIB etching. The differences in tunnel widths resulted in differences in tunnel resistances. The difference in the island size resulted in the difference in the capacitance of the device, hence, the charging energies. The conductance of the SET in the strong tunneling regime was calculated for different tunnel resistances. It was observed that the effect of tunnel resistance on the conductance of the SET was the dominant factor compared to the charging energy of the system. The experimental results obtained confirm the theoretical calculations of conductance of the SET in the strong tunneling regime. The fabricated devices had tunnel resistances of  $5k\Omega$  for a tunnel width of 20nm, and a tunnel resistance of  $22k\Omega$  for a tunnel width of 30nm. This difference in the fabricated structures resulted in differences in the device parameters, and therefore, in the conductance of the device. The conductance of the SET

can be controlled by varying the tunnel junction width of the SET. The minimum island size fabricated using FIB etching was found to be 40nm, and the minimum tunnel junction width was found to be 20nm. because of the large diameter of the conducting island, and also because of the lower value of tunnel junction resistance, room temperature operation of the device cannot be observed.

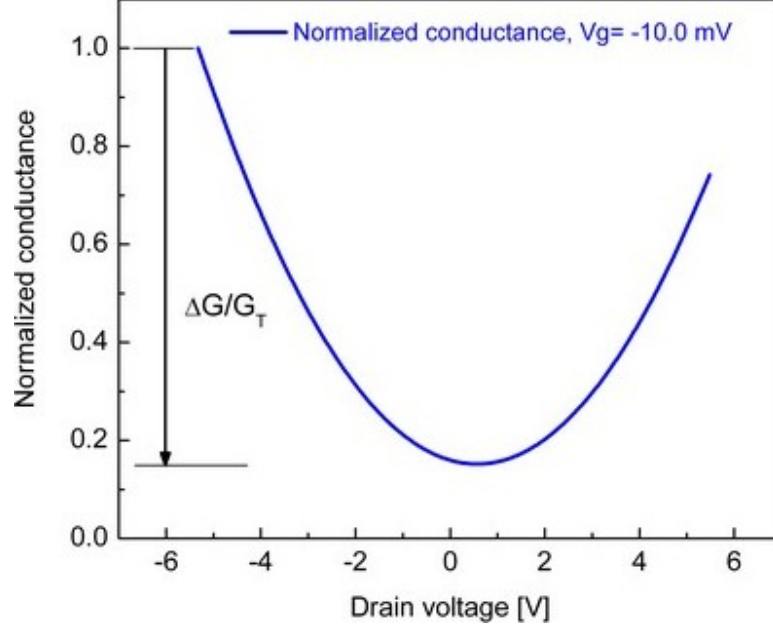


## 5.2 Device parameter extraction

The device parameters of a single dot SET system can be extracted using the orthodox model. For a multiple-junction device, the device parameters can be calculated from the measured data using "orthodox theory". [75] Utilizing the measured average size of the nano islands ( $\sim 8$  nm) and the spacing between source and drain terminals, It is estimated that the device consists of an array of 20 tunnel junctions, or ten conducting islands. Assuming that the tunnel junctions within the SET device have the same resistance and capacitance, the charging energy of the device is calculated according to the Equ. (5.2)

$$\frac{\Delta G}{G_T} = \frac{E_C}{3\kappa_B T} \frac{(N-1)}{N} \quad (5.2)$$

[76], Where  $E_C$  is the charging energy  $E_C = \frac{e^2}{2C}$ ,  $C^*$  is the capacitance of the array and  $N$  is the number of junctions in the array,  $G$  is the dip in the measured conductance around zero source-drain bias of the device and  $G_T$  is the asymptotic conductance at large positive and negative source-drain bias of the device measured . The capacitance per junction  $C$  is related to the total capacitance  $C^*$  as  $C^* = \frac{NC}{2(N-1)}$  . The dip in the normalized conductance as measured from the conductance of the device is calculated from the differential conductance of the source-drain characteristics of the device. Using the normalized dip in the conductance of the device and



**Figure 5.4:** Dip in the conductance of the of the device.

the above equations the charging energy is calculated. Using the charging energy the effective capacitance,  $C^*$ , of the device is obtained, and then, the capacitance of the individual junction is calculated. The resistance of the tunnel junctions, which is related to the charging energy, the temperature of operation and the number of tunnel junctions in an array is calculated. The dip in the normalized conductance of one of the SET device is shown in the Figure 5.4.

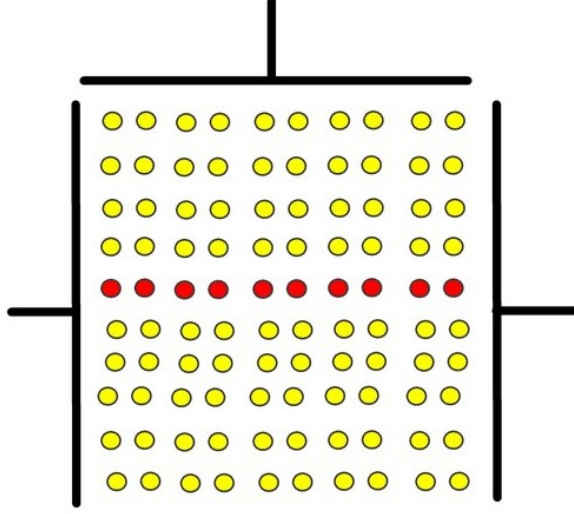
The graph shows the normalized differential conductance of the SET device,  $\frac{\Delta G}{G_T}$  is the dip in the normalized conductance of the device. Device parameters for all the different device configurations, of the devices have been extracted, using the experimental coulomb blockade characteristics of the device. The differential conductance of the device have been calculated from the coulomb blockade characteristics, then the nor-

malized differential conductance of the device is extracted. The device characteristics of the devices are shown in the Table 5.1.

**Table 5.1:** Device parameters for the SET devices

Device	Dip in Conductance	$E_C[meV]$	$C_{eff}[aF]$	$C[aF]$	$R[G\Omega]$
DT1 Pre-island (d11)	0.85	150.6	0.53	1.090	39.78
DT1 Post-island (d12)	0.97	180.0	0.45	0.952	25.58
DT2 Pre-island (d23)	0.94	169.7	0.47	0.985	29.20
DT2 Post-island (d24)	0.877	154.6	0.52	1.056	36.51
DT3 Pre-island (d15)	0.968	179.2	0.45	0.958	26.24
DT3 Post-island (d26)	0.974	152.8	0.52	0.950	26.00

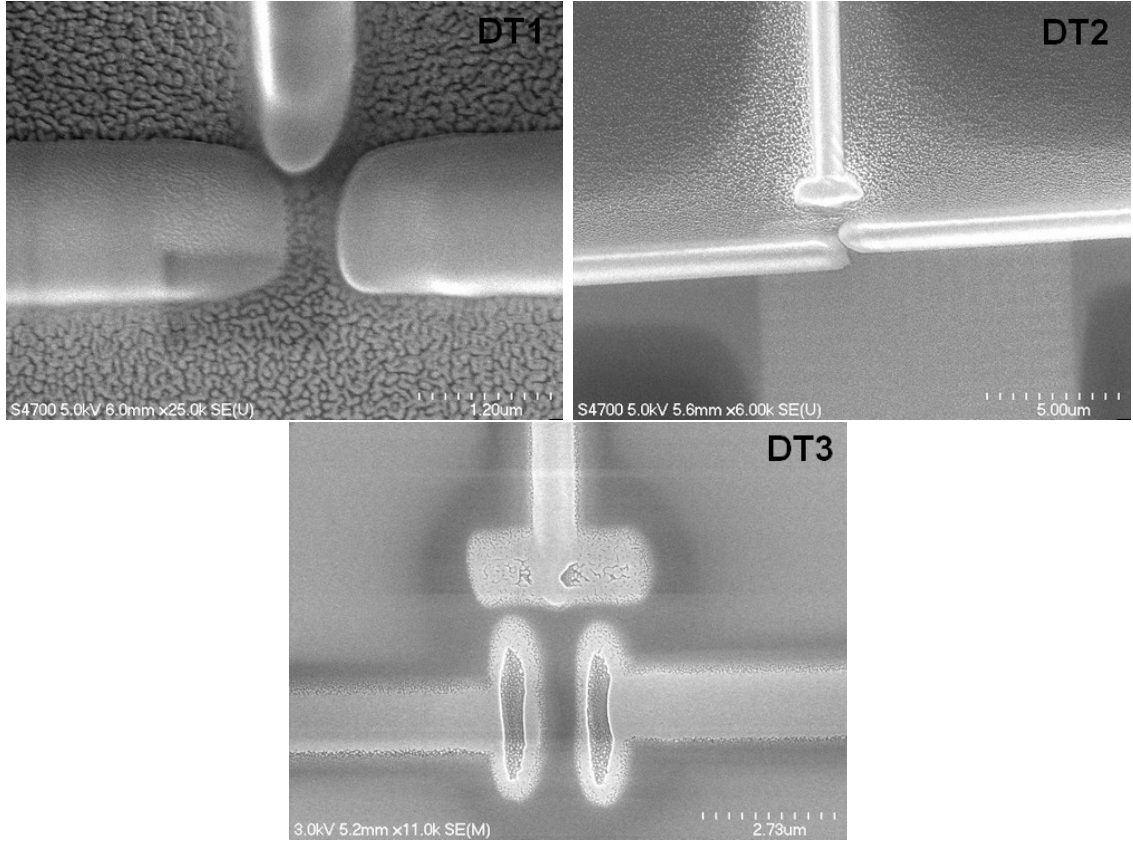
The effective capacitance obtained from the parameter extraction, does not include the gate capacitance. The gate electrode is acting on all the conducting islands present in between the source drain terminal. Based on the dimensions of the source drain terminals and the dimensions of the conducting island, it is estimated that, there are an array of  $10 \times 10$  nano-islands. The soliton model assumed the linear array of tunnel junctions participating in the conduction process [75]. Hence only ten conducting nano-islands participate in the conduction process, and gate capacitance of ten nano-islands should be considered for the total capacitance of the device. The pictorial image of the device configuration shows one such possible tunnel event in Figure 5.5. The effective capacitance and the gate capacitance are combined in series to obtain the total capacitance of the device.



**Figure 5.5:** Gate Capacitance of the of the device.

### 5.3 Comparison of different device configurations

Device configurations presented, have different device parameters. The difference in the device parameters are due to the differences in the geometrical arrangement of the active nano electrodes, which have a dominant effect on the transport characteristics of the device. The SEM micrographs of the fabricated device structures are shown in the Figure 5.6. The differences in the arrangement of the electrodes will impact the gate capacitance, and hence, the overall capacitance of the device. The overall capacitance of the device determines the charging energy of the device. The electric fields perceived by the conducting nano-islands are different, based on the arrangement of the electrodes. The applied fields, in the source-drain direction, and the field between the conducting nano-islands and the gate terminal can be varied by the inclusion of



**Figure 5.6:** SEM micrographs of different Device configurations.

the nano-electrodes at the end of the source, drain and gate terminals. The following sections explore the differences in the device characteristics, based on the geometrical variations of the active electrodes.

### 5.3.1 Pre-island fabricated devices

The device parameters are extracted using the experimental device characteristics. The extracted device parameters for the pre-island fabricated SET devices are presented in Table 5.2. The non linear device characteristics for all the different device configurations for the pre island fabricated SET devices are presented in the Fig 5.7. The coulomb blockade length of the SET device, is dependent on the effective capacitance of the device. The effective capacitance of the device is made up of the capacitance of the islands, the capacitance of the tunnel junctions, and the capacitance of gate electrode. The effective capacitance of the device is extracted using the device parameter extraction model as explained in section 5.2, the extracted effective capacitance does not include the gate capacitance. The total capacitance of the device is the series combination of the effective capacitance, and the gate capacitance acting on the conducting nano-islands.

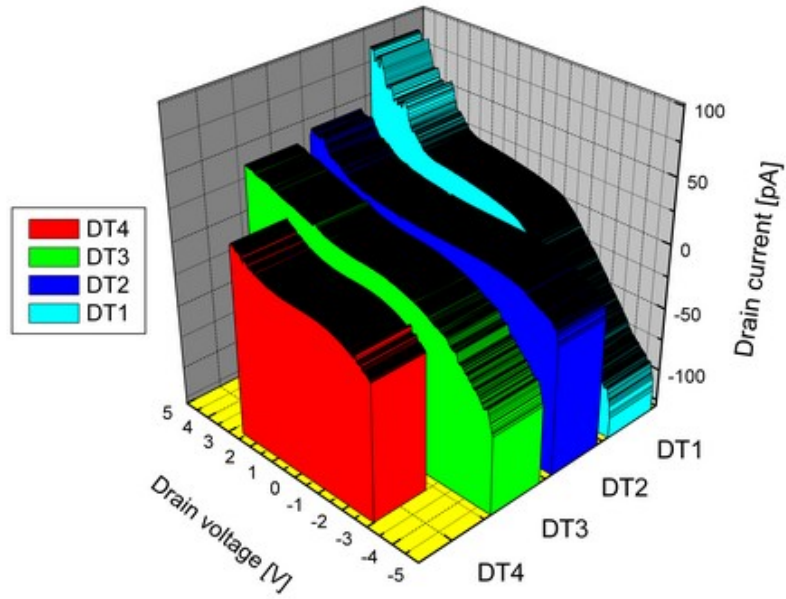
**Table 5.2:** Device parameters for the pre-island fabricated SET devices

Device	Dip in Conductance	$E_C[meV]$	$C_{eff}[aF]$	$C[aF]$	$R[G\Omega]$
DT1	0.84987	150.6	0.532	1.0905	39.786
DT2	0.94048	169.7	0.472	0.9854	29.2
DT3	0.9676	179.2	0.447	0.9578	26.244
DT4	0.978	167.5	0.478	0.947	25.13

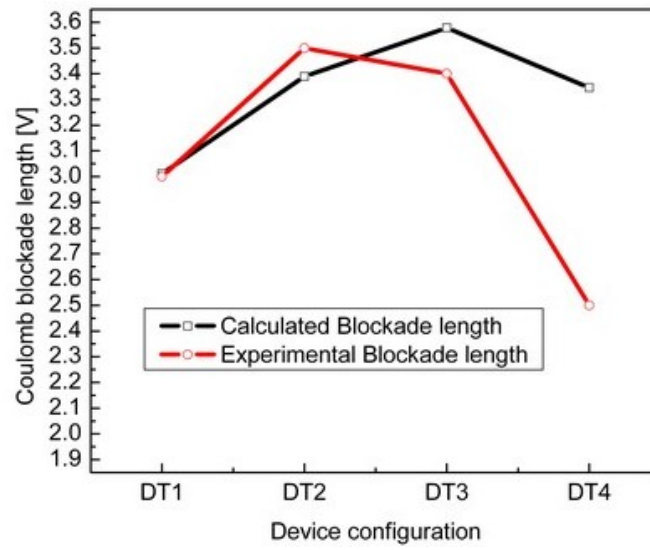
The coulomb blockade of the SET device is the region where there is no increase in the drain current for an increase in the source drain voltage. The blockade of the device is dependent on the total capacitance of the device. It can be observed from

Figure 5.7, that the blockade lengths for device configurations are different. The blockade characteristics are observed within the source-drain sweep of -6.0 V to 6.0 V. The coulomb blockade length calculated from the effective capacitance of the device, and the coulomb blockade length observed from the device characteristics are compared in the Figure 5.8. The coulomb blockade length observed from the experimental data is in agreement with the calculated coulomb blockade length. The blockade length varies from 3.0 V to 3.6 V, hence it can be concluded that the geometry of the nano conducting leads would influence the over all capacitance of the device and in turn the coulomb blockade of the device. The device configurations DT1 to DT4 can be used to modulate the blockade length. The maximum drain current observed for these configurations with pre island fabricated islands are in the range of few tens of pico-Amps.

The effective capacitance of the device configurations decrease from configuration DT1 to DT3, and the capacitance for the configuration DT4 increases. The addition of the nano structures perpendicular to the connecting electrodes, reduces the capacitance of the device. The introduction of the parallel plate geometry at the end of the source drain terminals, along with the presence of the gate terminal was found to reduce the capacitance of the device, as shown in the Figure 5.9. The charging energy for the device configurations was found to increases from 150.6 meV to 179.2 meV from DT1 to DT3, for DT4 the charging energy decreases 167.5 meV. The charging energy and the total capacitance of the device are reciprocal to each other. It can be concluded,

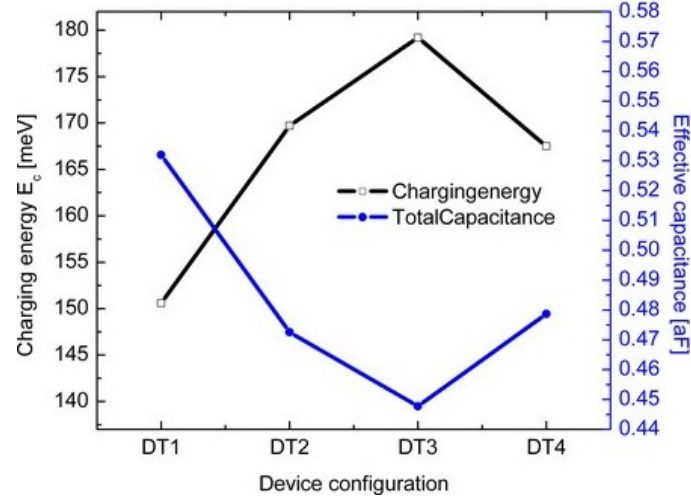


**Figure 5.7:** Non linear characteristics of the SET devices with Pre fabricated island

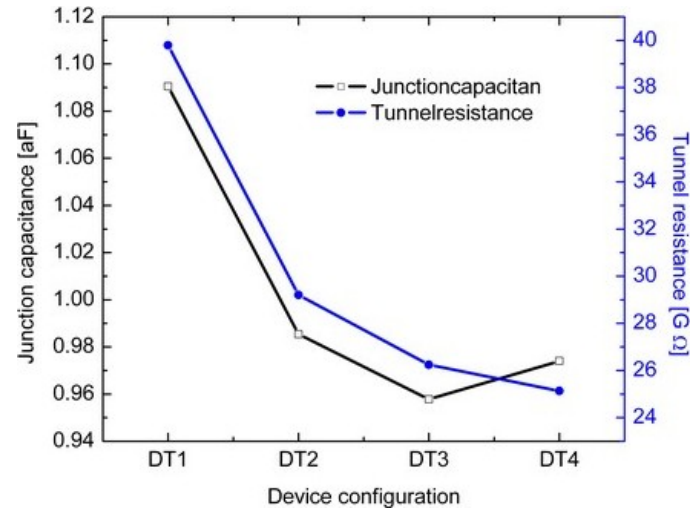


**Figure 5.8:** Coulomb blockade comparison for Pre fabricated island fabricated device





**Figure 5.9:** Charging energy and effective capacitance of pre island fabricated SET structures



**Figure 5.10:** Tunnel resistance and capacitance per junction of pre island fabricated SET structures

that, reduction in the dimensions of the connecting nano-electrodes, would reduce the total capacitance and, hence would improve the charging energy of the device.

The tunnel resistance of the device configurations decrease from DT1 to DT4 from

$40G\Omega$  to  $25G\Omega$ . The higher the tunnel resistance, the higher is the confinement of electrons to the conducting islands. It can be concluded that the introduction of the nano-structures in the active area of the device would reduce the tunnel resistance of the device. The junction capacitance of the device also decreases with the introduction of the nano-structures in the active area of the device, as shown in Figure 5.10.

### 5.3.2 Post-island fabricated devices

The device parameters are extracted using the experimental device characteristics. The extracted device parameters for the post-island fabricated SET devices are presented in Table 5.3. The non linear device characteristics for all the different device configurations for the post island fabricated SET devices are presented in the Figure 5.11. The coulomb blockade length of the SET device, depends on the effective capacitance of the device. The total capacitance of the device is the series combination of the effective capacitance, and the gate capacitance acting on the conducting nano-islands. The coulomb blockade length of different device configurations from DT1 to DT3 increase from 5.0 V to 8.0 V, as observed experimentally, but the theoretically calculated blockade lengths are from 3.5 V to 3.05 V.

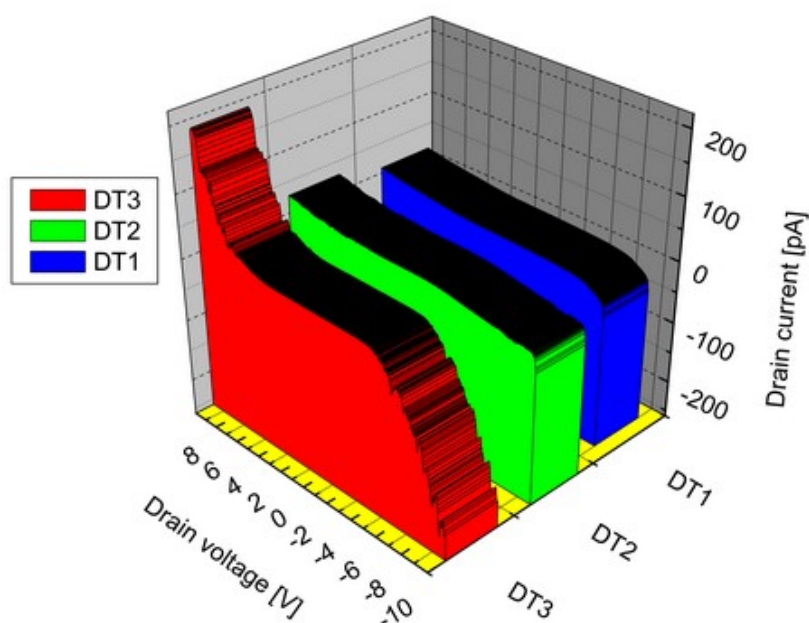
**Table 5.3:** Device parameters for the post-island fabricated SET devices

Device	Dip in Conductance	$E_C[meV]$	$C_{eff}[aF]$	$C[aF]$	$R[G\Omega]$
DT1	0.84987	180.0	0.5009	1.0905	25.582
DT2	0.94048	154.6	0.5562	0.9854	36.51
DT3	0.9676	152.8	0.5812	0.9578	41.107

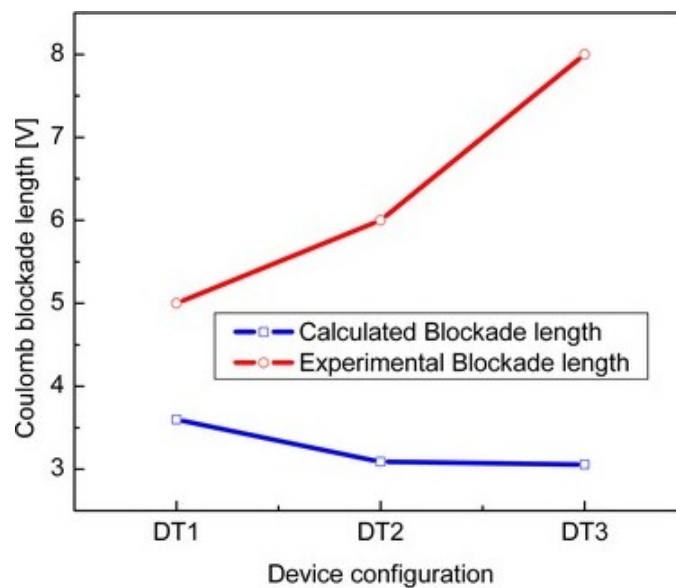
The blockade of the device is dependent on the total capacitance of the device. It can be observed from Figure 5.11, that the blockade lengths for device configurations are different. The blockade characteristics are observed within the source-drain sweep of -12.0V to 12.0 V. The coulomb blockade length calculated from the effective capacitance of the device, and the coulomb blockade length observed from

the device characteristics are compared in the Figure 5.12. The coulomb blockade length observed from the experimental data is not in correlation with the calculated coulomb blockade length. One of the reasons for this behavior is that, the calculated capacitance does not include any contribution from the  $Al_2O_3$  passivating layer. It is believed that the capacitance from the passivating layer is acting in series to the device capacitance and reducing the total capacitance of the device. This would increase the coulomb blockade length of the post island fabricated devices. The blockade length varies from 5.0 V to 8.0 V, hence it can be concluded that the geometry of the nano-conducting leads would influence the overall capacitance of the device and in turn the coulomb blockade of the device. The device configurations DT1 to DT3 can be used to modulate the blockade length. The maximum drain current observed for these configurations with post island fabricated islands are in the range of few hundreds of pico-Amps, which is an order of magnitude higher than the pre island fabricated devices.

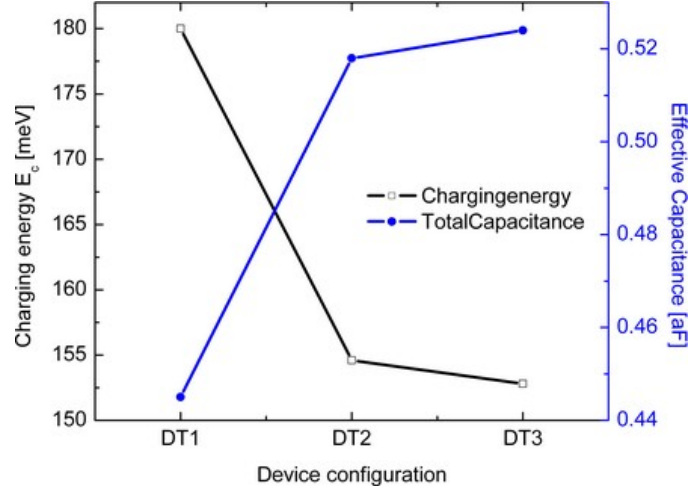
The effective capacitance of the device configurations increase from configuration DT1 to DT3. The addition of the nano-structures perpendicular to the connecting electrodes, increases the capacitance of the device. The introduction of the parallel plate geometry at the end of the source drain terminals, along with the presence of the gate terminal was found to increase the capacitance of the device, as shown in the Figure 5.13. The charging energy for the device configurations was found to decrease from 180.0 meV to 152.8 meV from DT1 to DT3. The charging energy and



**Figure 5.11:** Non linear characteristics of the SET device configuration DT1 Post fabricated island



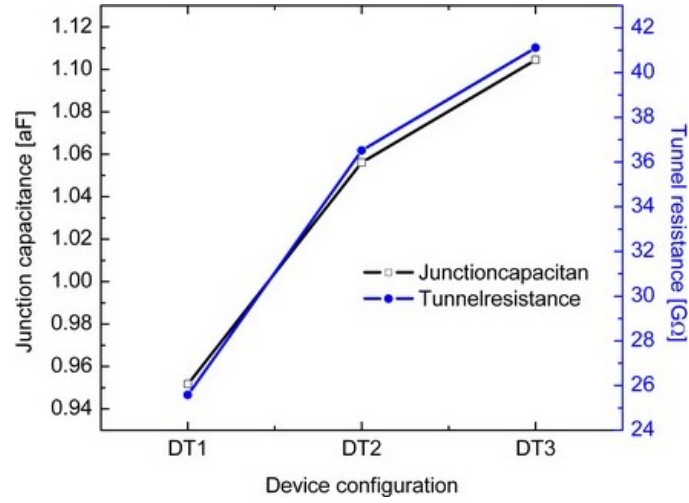
**Figure 5.12:** Coulomb blockade comparison for Post fabricated island fabricated device



**Figure 5.13:** Charging energy and effective capacitance of post island fabricated SET structures

the total capacitance of the device are reciprocal to each other. It can be concluded, that, reduction in the dimensions of the connecting nano electrodes, would increase the total capacitance and, hence would reduce the charging energy of the device. The device behavior, of the post island fabricated devices is opposite to that of the pre fabricated device structures. The reason for such device behavior is that, the oxidation of post fabricated device structures, would form an oxide layer, encapsulation the nano leads and the conducting nano islands. This would minimize the interaction of the  $Al_2O_3$  passivating layer, and hence will result in the reduction of the total capacitance of the device.

The tunnel resistance of the device configurations increases from DT1 to DT3 from  $25.58G\Omega$  to  $41.107G\Omega$ . The higher the tunnel resistance, the higher is the confinement of electrons to the conducting islands. It can be concluded that the introduction of



**Figure 5.14:** Tunnel junction resistance and capacitance per junction of post island fabricated SET structures

the nano-structures at in the active area of the device would increase the tunnel resistance of the device. The junction capacitance of the device also increases with the introduction of the nano-structures in the active are of the device, as shown in Figure 5.14.

## 5.4 Model verification

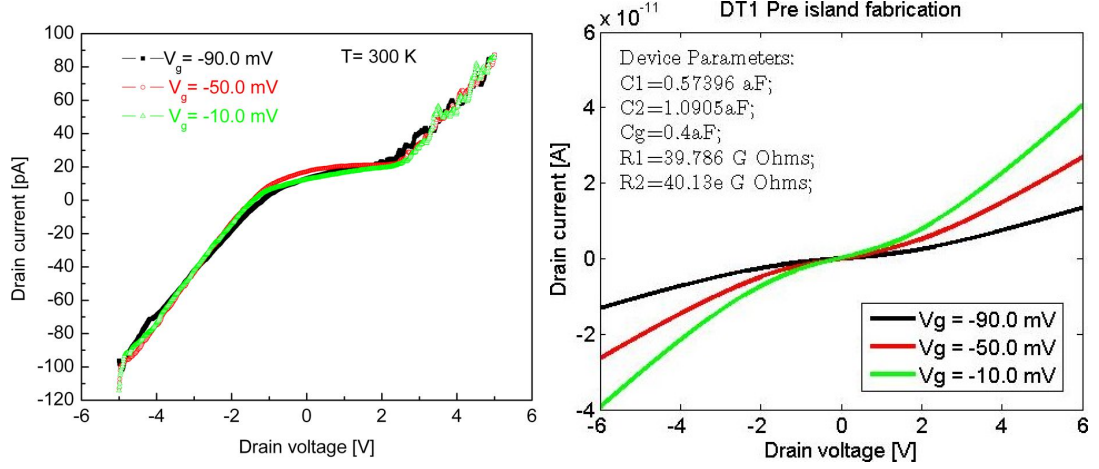
The non-linear Coulomb blockade characteristics of the multi dot SET device can be explained using the Soliton model [77] as explained in section 2.3. The source drain non linear characteristics for different device configurations have been simulated. The device parameters used in the simulation are obtained from the experiment, which are extracted using the device parameter extraction, as explained in section 5.2. The theoretical simulations of the device characteristics for different device topologies have been investigated. The device characteristics for pre-island fabrication process and post-island fabrication process were obtained as shown in Figures 5.15, 5.16, 5.17 and Figures 5.18, 5.19, 5.20 respectively . Differences in the device characteristics were observed for different device topologies. The capacitance of device configurations varied, because of the differences in the active electrode configuration of the device. The Table 5.4 presents the ratio of the tunnel junction resistances and capacitances used in the device simulation. The device parameters used in the simulation were modified from the experimentally extracted device parameters to match the device data. With the data used in simulations, it was observed that, the shape of the device characteristics, along with the coulomb blockade length of the device was captured by the present model. The obtained drain current was in agreement with the experimental data. Hence can be concluded that the model can be used to predict the coulomb blockade length and the magnitude of the drain current of the device.



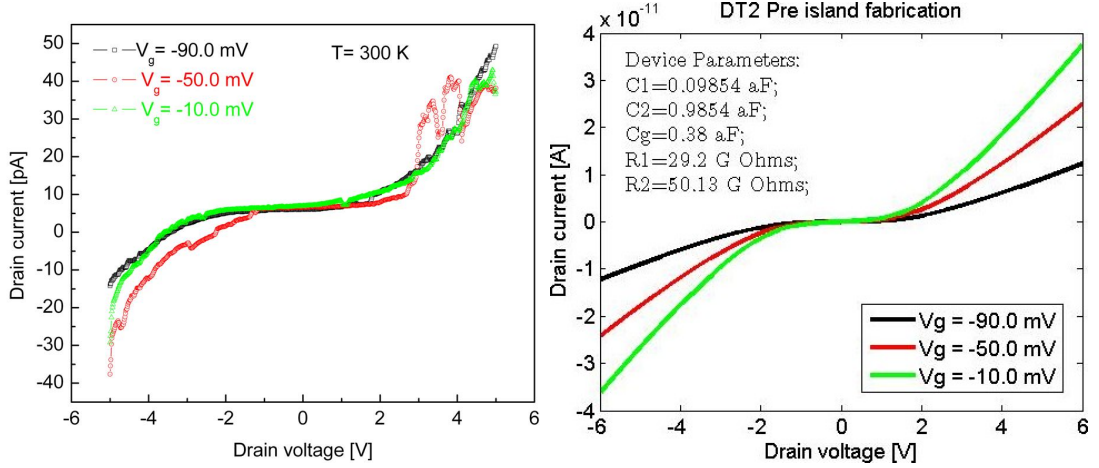
The model assumes that the tunnel junction resistance on both sides of the junction  $R_1$ , and  $R_2$ , are same for all the conducting islands, which is not the case in the practical device. It can be seen that, when the ratio of  $R_1/R_2$  and  $C_1/C_2$  decreases, the coulomb blockade length of the device increases, for the pre island fabricated devices. The smaller asymmetry in the tunneling properties of the junctions, result in larger coulomb blockade, and a large asymmetry in the tunneling properties of the junctions, result in smaller coulomb blockade. Physical reason for the reduction in the blockade length of the device is the reduction in the total capacitance of the device, which, occurs at lower asymmetric tunnel junctions. The model also assumes that the conduction of electrons is along a linear array of tunnel junctions, which might not be the case depending on the electrostatics of the system. Hence the limitations of the present model is that, the model does not capture the higher voltage effects, which are seen in the experimentally obtained data.

**Table 5.4:** Model verification for pre-island fabricated SET devices

Device configuration	$R_1/R_2$	$C_1/C_2$	$C_g[aF]$
DT1	0.99	0.526	0.4
DT2	0.582	0.1	0.38
DT3	20.717	1.593	0.459

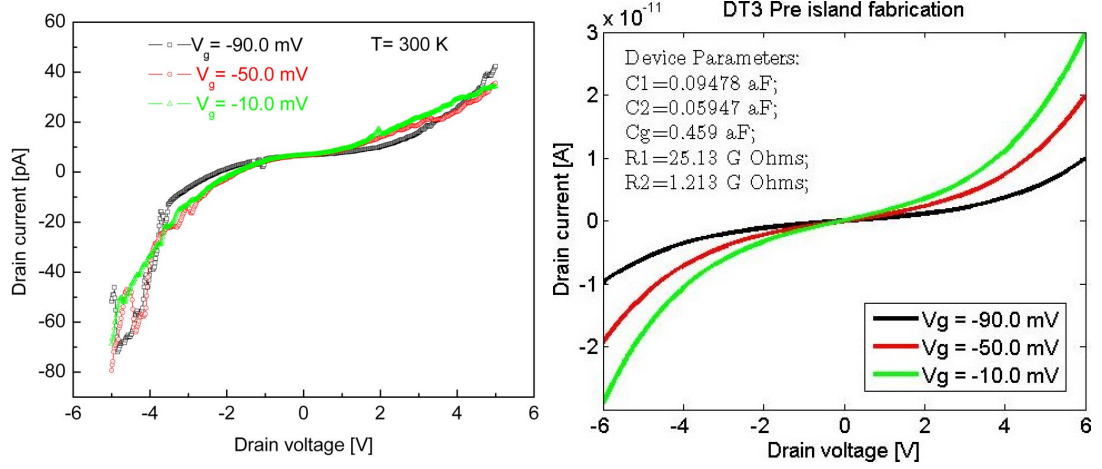


**Figure 5.15:** Experimental(left) and theoretical non linear  $I$ - $V$  characteristics of device DT1



**Figure 5.16:** Experimental(left) and theoretical non linear  $I$ - $V$  characteristics of device DT2

Comparing the experimental data with the simulated source drain characteristics, it can be observed that, the trend of the coulomb blockade is maintained. The average current calculated is in the range of pA showing that the present model is capable of extracting the source drain characteristics of the multidot SET device. The



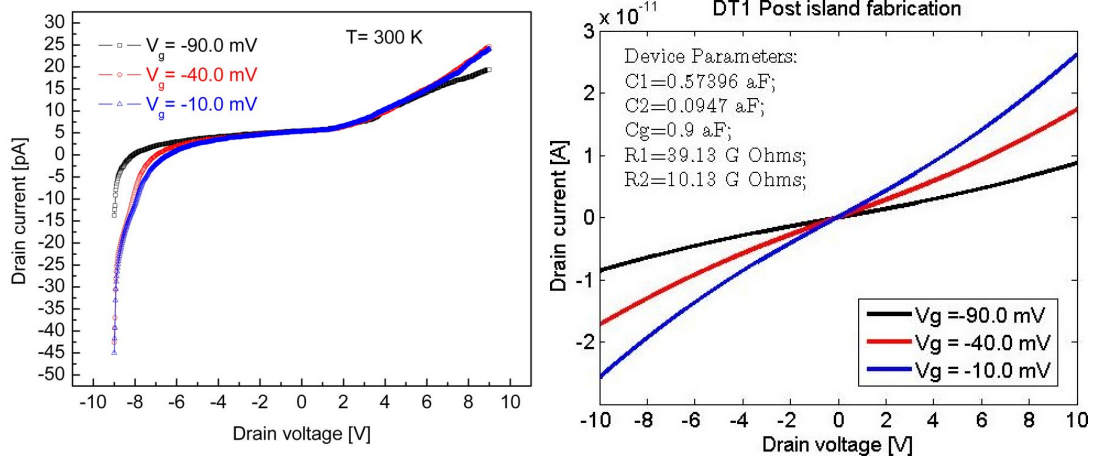
**Figure 5.17:** Experimental(left) and theoretical non linear  $I$ - $V$  characteristics of device DT3

inclusion of the extra terminal on the gate electrode increased the capacitance. The gate capacitance is assumed to be made up of individual capacitances acting on the conducting islands in parallel. The gate capacitance acting on individual conducting island is decreased from device configuration DT1 to DT2 from  $0.4 \text{ aF}$  to  $0.038 \text{ aF}$ , and found to increase to  $0.459 \text{ aF}$  for DT3 pre island fabricated structures and, found to decrease from  $0.9 \text{ aF}$  to  $0.034 \text{ aF}$  for, the device configurations DT1 to DT3, in case of the post island fabricated structures.

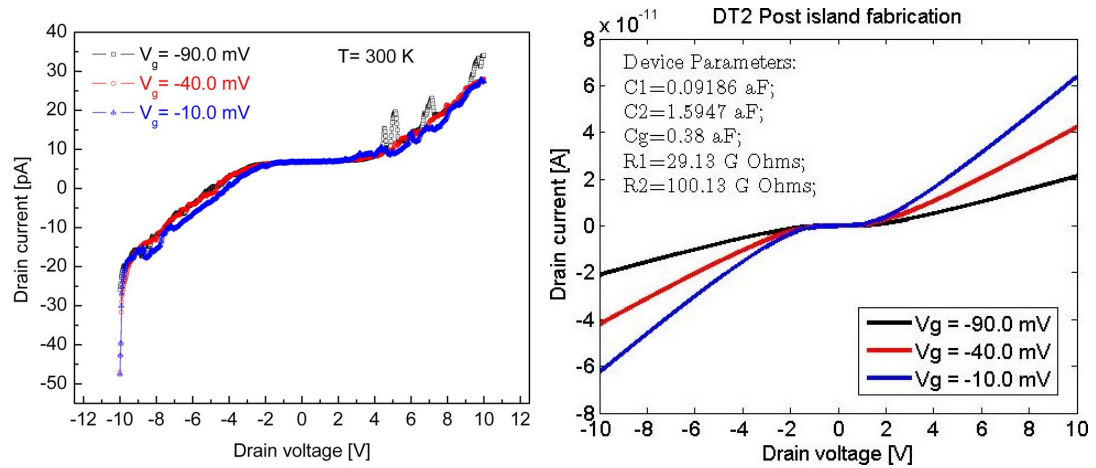
**Table 5.5:** Model verification for post-island fabricated SET devices

Device configuration	$R_1/R_2$	$C_1/C_2$	$C_g[\text{aF}]$
DT1	3.862	6.060	0.9
DT2	0.290	0.0576	0.38
DT3	2.168	1.6105	0.034

The simulated source drain characteristic do show Coulomb blockade effect, but does



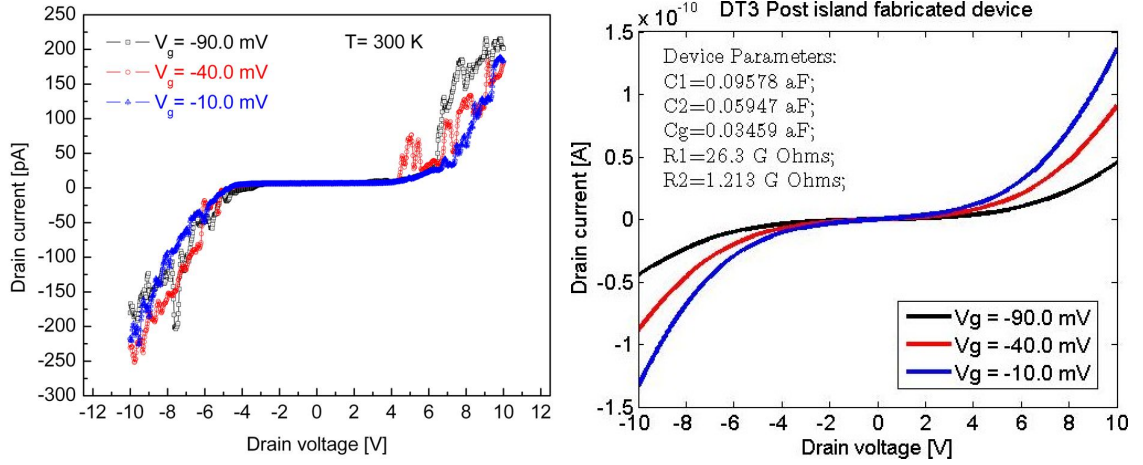
**Figure 5.18:** Experimental(left) and theoretical non linear  $I-V$  characteristics of device DT1 Post fabricated island.



**Figure 5.19:** Experimental(left) and theoretical non linear  $I-V$  characteristics of device DT2 Post fabricated island.

not shown the Coulomb staircase effect at higher source drain voltages. Some of the reasons attributed for not capturing the staircase effect in the device characteristics are the following.

1. The model assumes that the conduction of electrons is via a linear array of



**Figure 5.20:** Experimental(left) and theoretical non linear  $I$ - $V$  characteristics of device DT3 Post fabricated island.

tunnel junctions.

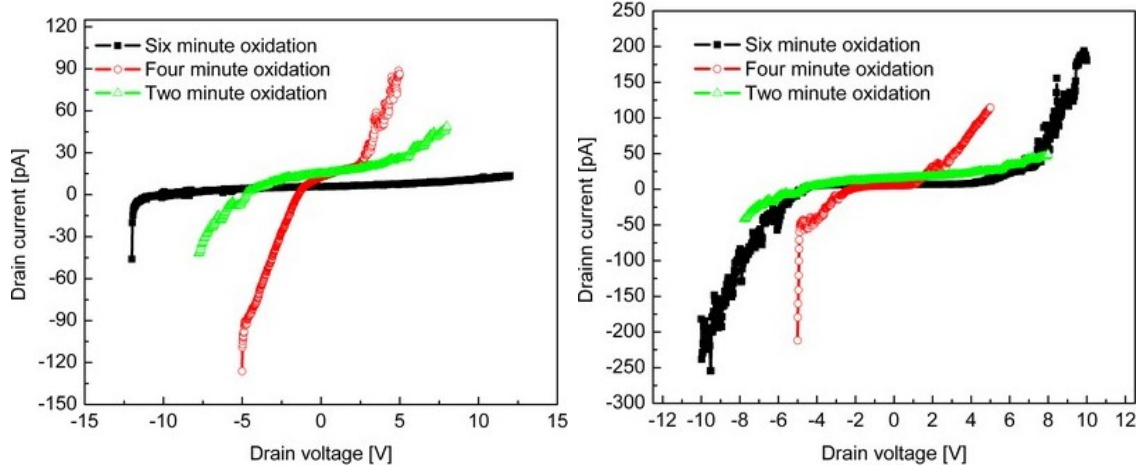
2. The assumed parameters of the tunnel junctions  $R_1$ , and  $R_2$  are taken to be equal, which is not the case in the practical device.
3. The assumed parameters of the tunnel junctions  $C_1$ , and  $C_2$  are taken to be equal, the island size variations in the device will lead to different capacitances of the tunnel junctions.
4. The differences in the spacing between the island because of a small change in the island size would lead to the difference in the tunnel resistances of the tunnel junctions.
5. The inter island capacitance interactions are not taken in to account in the model and hence would lead to loss of fine structures which are observed at higher source drain voltages in the practical device.

The Soliton model is semi classical in nature, and does not take the variation in tunnel junction properties into account. The incorporation of the variation of the tunnel junction properties for each junction in the model, along with the inclusion of the inter capacitances between the islands, would improve the model.

## 5.5 Tunnel junction modulation effects on the Device Characteristics

Tunnel junctions for the SET device are fabricated using the chemical oxidation of tungsten in peracetic acid. The oxidation time determines the thickness of the tungsten oxide formed. The thickness of the tungsten oxide plays an important role in the device characteristics of the SET device. The tunnel resistance of the device is determined by quality of the tunneling oxide. The present section shows the modulation of device characteristics, in particular the blockade voltage with the thickness of the tunneling oxide. Three different oxide thickness were considered, for the investigation of the effects of oxide thickness on the device characteristics. The thickness again depends on the oxidation times, in this case two minutes, four minutes and six minutes were considered (Thickness based of the oxidation times would be updated, experiments are in progress to extract the thickness of the oxide). Two different device topologies DT1 and DT3 were investigated.

The effect of oxide thickness on the device characteristics of configuration DT1 are shown in Figure 5.21. It is very clear that the blockade voltage is different for different oxide thickness. It is observed that for the oxidation time of six minutes, the blockade voltage is the largest at 9.0 V, and the blockade voltage is 4.0 V the minimum at the oxidation time of four minutes. The blockade voltage of the device is dependent on the effective capacitance of the device, with the change in the oxide thickness, the

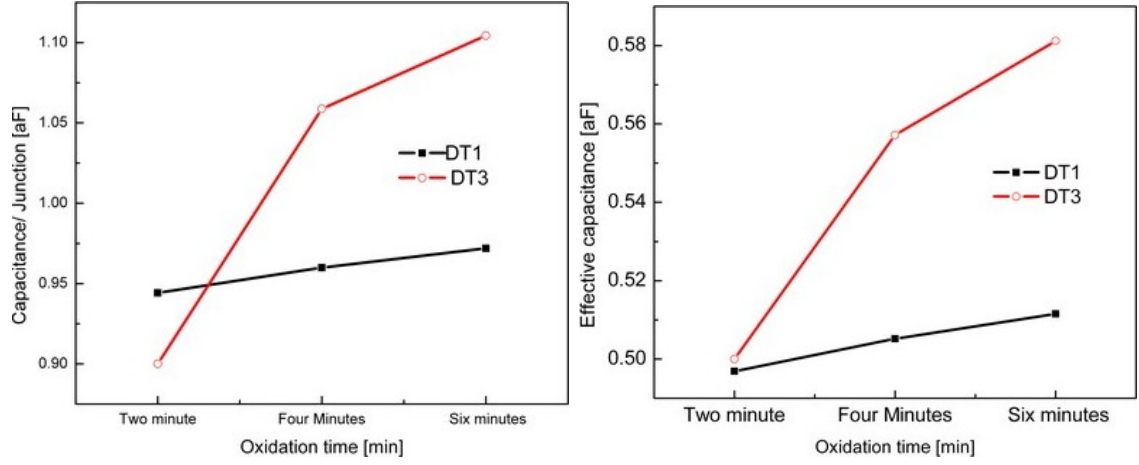


**Figure 5.21:** Effect of oxide thickness on configuration DT1 and DT3 respectively.

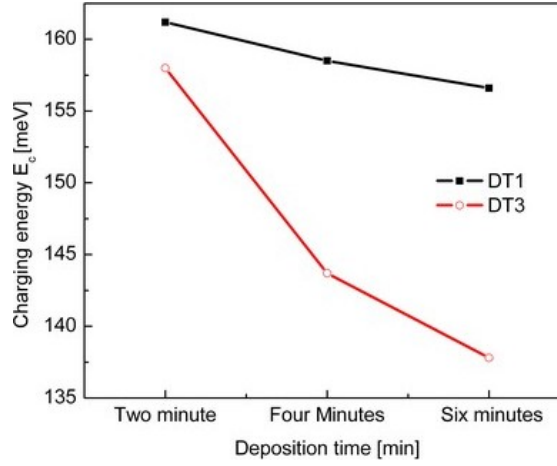
effective capacitance of the device is also changed, thus contributing to the blockade voltage. A similar trend is observed in the blockade lengths of the device DT3. The differences in the blockade voltage between the two device configurations is due to the fact that differences in the device configuration would contribute to the change in the effective capacitance of the device.

The charging energy is given by  $E_C = \frac{e^2}{2C}$ , which depends on the effective capacitance. The junction capacitance depends on the geometrical structure of the electrode and the material properties of the tunnel junction oxide. The tunnel resistance of the device is also related to the charging energy. It was observed that the junction capacitance per junction increased with the oxidation times of the oxide (Decrease in the oxide thickness). The increase in the capacitance was consistent with different device configurations. The increase in junction capacitance would contribute to the increase in





**Figure 5.22:** Oxide thickness effect on the capacitance of configuration DT1 and DT3 respectively.



**Figure 5.23:** Charging energy of the device.

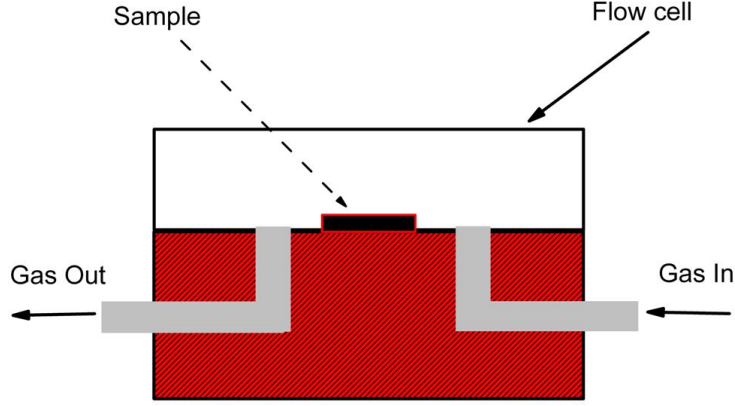
the effective capacitance of the device, as shown in Figure 5.22. The charging energy of the device depends on the effective capacitance of the device, and as the effective capacitance increase with the oxidation times, the charging energy of the device decreases with the (decrease in the oxidation thickness), as shown in Figure 5.23.

## 5.6 Applications of Single Electron Transistors

Room temperature operating single electron transistor can be used as very sensitive electrometer. The gate electrode of the SET is used as the sensing electrode. The adsorption of the gas molecules on the gate electrode, induce extra charge on the gate terminal and hence, modulate the device characteristics. The sensing mechanism is based on the modulation of the charge on the gate electrode because of the interaction of the gas species with the surface complexes present on the gate electrode. The adsorption of the gas species to the surface complexes changes the charge state of the gate electrode resulting in a change in potential on the tunneling junctions, hence results in the change in electrical conductivity of the SET. The present section investigates the room temperature SET as a gas sensor, and applied for the sensing of  $N_2O$  gas.

### 5.6.1 SET as Gas Sensor

In metal oxide based gas sensing systems, the sensing mechanism is dependent on the changes induced in the electrical properties of the sensing film. The electrical changes induced are due to the interaction between the surface complexes of the sensing film and the molecules of the sensing species to be detected. The chemical species adsorbed near the grain boundaries of the sensing film affect the electronic transport of the gas sensor. The low surface to volume ratio, hampers the sensitivity of such

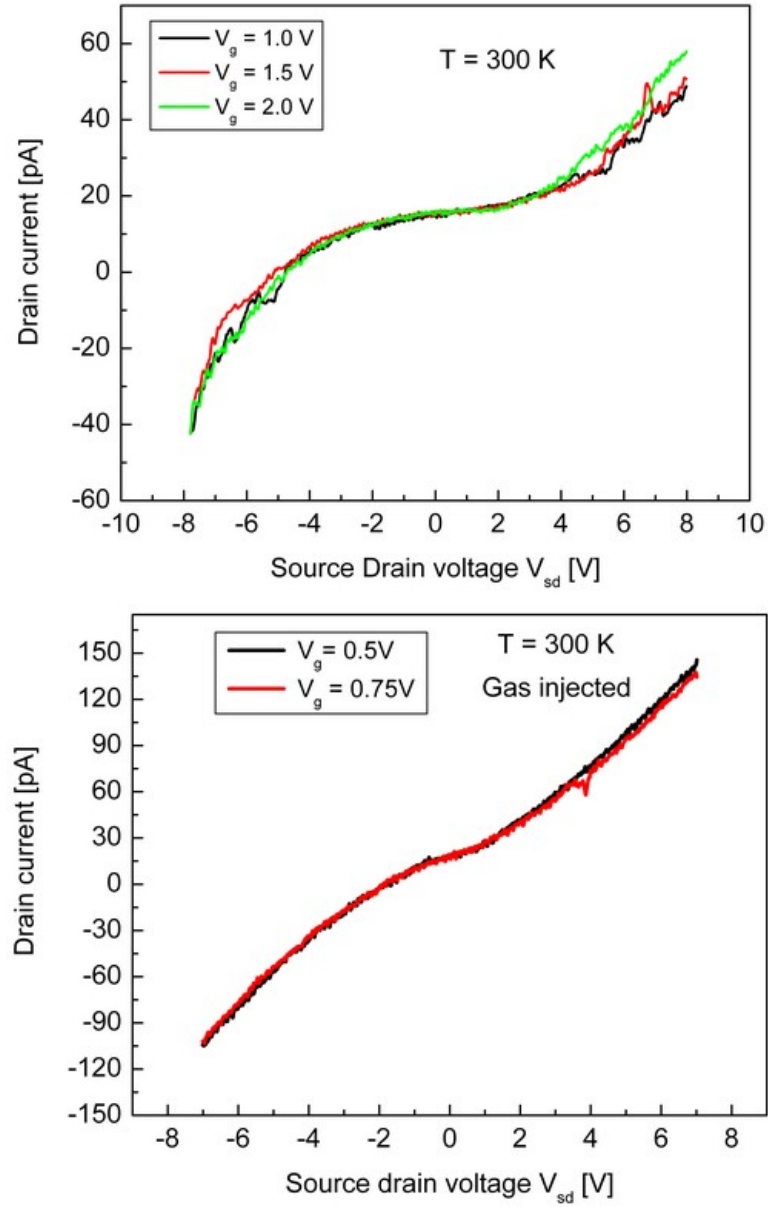


**Figure 5.24:** Cross sectional view of the flow cell. .

devices [78]. High surface to volume ratio can be achieved in one dimensional nanostructures and nano islands, which would exhibit high sensitivity and fast response times [79; 80]. Overall, sensing films with high surface to volume ratios can enhance sensitivities to adsorbed species [81], [82], [83]. In this application, a single electron transistor is utilized as a  $N_2O$  gas sensor. The SET sensor is fabricated using a focused ion beam deposition process utilizing tungsten nano particles as conducting islands and tungsten nano leads and connecting pads. Charge applied to the gate electrode results in a modulation of the electron transport through the tunneling islands of the SET.  $N_2O$  gas sensing with different concentrations were investigated. With the incorporation of the gas, variations in the source drain characteristics of the SET device were observed. Reduction in the drain current by an order of magnitude was observed with the exposure to the  $N_2O$  gas. The reduction in the drain current, with appropriate gate bias shows an oscillatory behavior, showing that the sensitivity of the sensor can be tuned with the control of gate bias.

The gas sensing characteristics of the device are obtained by placing the SET device in a flow cell, which is shown in Figure 5.24. The flow cell allows for the constant flow of gas over the sample surface and also enabling the electrical connection for device measurements. The device for testing was centered between the gas ports of flow cell. The flow cell was sealed after the insertion of the measuring probes for device characterization. The characteristic nonlinear  $I_d - V_{sd}$  characteristics of the SET device without any gas flow through the flow cell were obtained, with a fixed gate bias and a voltage sweep of source drain bias.

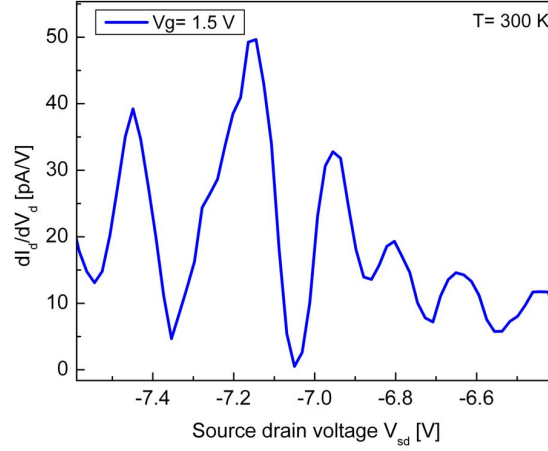
The SET characteristics with the flow of  $N_2$  gas through the flow cell were obtained with the same source drain bias and varying the gate bias. The incorporation of  $N_2O$  gas in to the flow cell with the constant flow of  $N_2$  gas as background was investigated with the SET device characteristics. The SET device was biased with 0.5 V between the source and drain terminals, and with different bias conditions on the gate terminal. The sensing characteristics of the device were obtained by varying the concentration of the  $N_2O$  gas in to the flow cell and obtaining the device characteristics. Concentration of the  $N_2O$  in  $N_2$  gas was varied from 36% to 100%. The drain current of the SET device was monitored with the injection of the mixture of  $N_2O$  gas and  $N_2$  gas. The injection of the gas species was detected by the SET by the variation in the drain current of the device. The drain current decreased by an order of magnitude with the injection of the gas species. Different concentrations of the  $N_2O$  gas resulted in variation of the reduction in the drain current, clearly



**Figure 5.25:** (a) A Coulomb blockade of 6 V is present at gate voltages of 1.0 V, 1.5 V and 2.0 V without gas injection, (b) Coulomb blockade of the SET device is reduced to 2 V with the injection of  $N_2$  gas into the flow cell.

showing the possibility of the detection of different concentrations of the  $N_2O$  gas species.

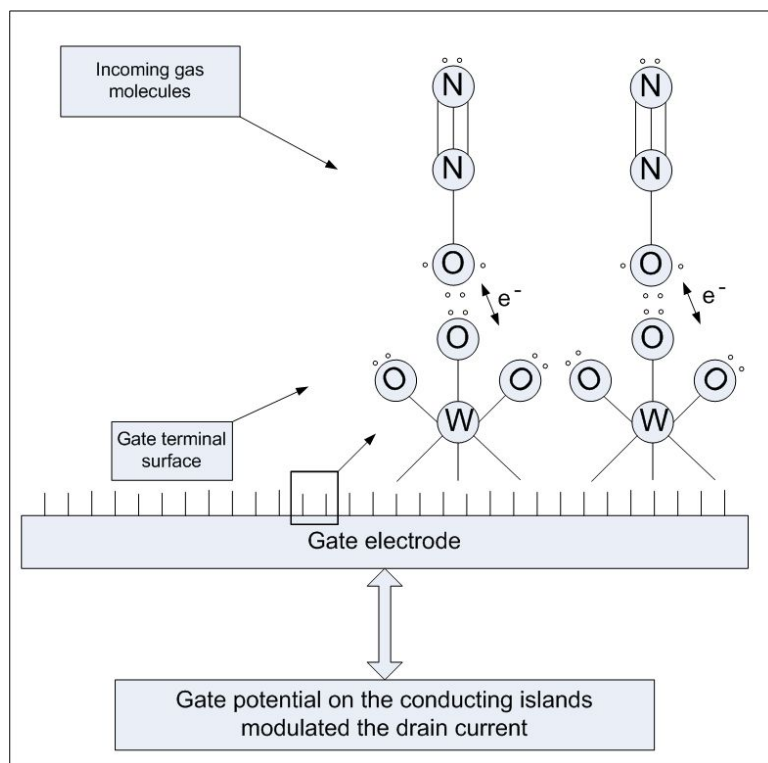
The nonlinear Coulomb blockade SET device characteristics for a fixed gate bias are shown in Figure 5.25. The blockade voltage was observed to be 6.0 V without the gas exposure to the SET device. With the exposure of the gas into the flow cell, the device characteristics resulted in the reduction of the blockade voltage to 2.0 V. The reduction in the blockade voltage of the SET is attributed to the increase in the overall capacitance of the device [84], which is due to the gas adsorption onto the tunneling oxide. The presence of gas on the electrode surface will affect the tunneling characteristics of the device by modulating the charge available on the gate terminal of the device, resulting in a modulation of the field present in the channel. The source drain current of the SET device was monitored with the incorporation of gas in to the flow cell. The drain current of the device was in the pico-Amperes range without the gas injection. The injection of the  $N_2$  gas resulted in the decrease in the drain current of the device.  $N_2$  gas has been reported for low temperatures to react with tungsten nano-particles generating  $N_2O$  gas [85]. We suspect that the tungsten nano-particles mediate the formation of adsorbed  $N_2O$  from the injected  $N_2$  (further investigation needs to be conducted), which in turns changes the charge state of the gate electrode. After the injection of a steady state  $N_2$  gas flow, the  $N_2O$  gas was injected in to the flow cell. The injection of  $N_2O$  gas resulted in the drain current drop of the SET device. The drain current reduction was by an order of magnitude. The gas is adsorbed on to the passivating  $Al_2O_3$  and also onto the gate terminal. The adsorbed gas on the gate electrode creates extra charge states which affect the



**Figure 5.26:** Clear Coulomb oscillations are present in the differential conductance of the SET.

transport of charge through the SET, and the gas adsorbed on the passivating oxide acts as a secondary gate applying charge, resulting in the modification of the SET device characteristics. The Coulomb oscillations in the differential current of the SET device is shown in Figure 5.26.

The gas was adsorbed on to the passivating  $Al_2O_3$  and the tungsten gate pad. The sensing mechanism was through ionosorption [86] of the gas molecules on the gate pad surface. The amorphous native tungsten oxide surface of the gate pad has an interatomic distance of 1.79 between tungsten and oxygen [87]. The number of available tungsten oxide sites for ionosorption of the incoming gas on a  $100\mu m \times 100\mu m$  pad was calculated to be approximately  $7.8 \times 10^{10}$ . The stable isotopic configuration expected for  $N_2O$  is N-N-O [88], and the number of electrons transferred between  $N_2O$  and the  $WO_3$  surface was calculated to be approximately  $1.56 \times 10^{11}$ , which is

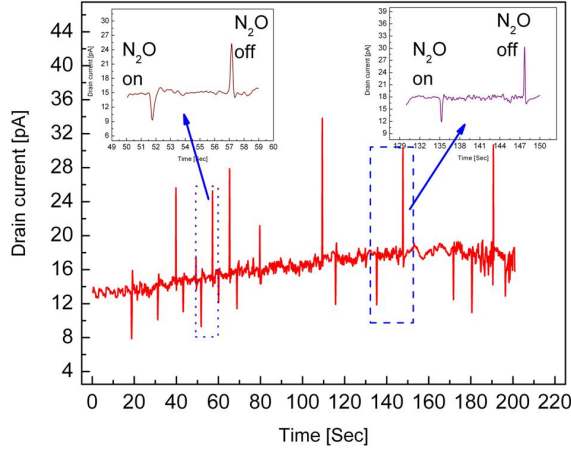


**Figure 5.27:** Proposed ionosorption mechanism resulting in charge transfer in the SET gas sensor.

in close agreement with the measured drop in the drain current. Depending on the surface state of the gate terminal and the incoming gas molecule, the electron transfer can be to the gate terminal or from the gate terminal. The removal of electrons from the gate terminal induces a positive bias on the gate, resulting in a downward spike in the drain current and vice versa. Figure 5.27 shows the proposed sensing mechanism of the SET gas sensor, where the incoming gas molecules are adsorbed on the gate surface, facilitating charge transfer. The charge transfer on the gate terminal modulates the drain characteristics of the SET device.

With the continuation of the gas flow the adsorption of the gas molecules on the



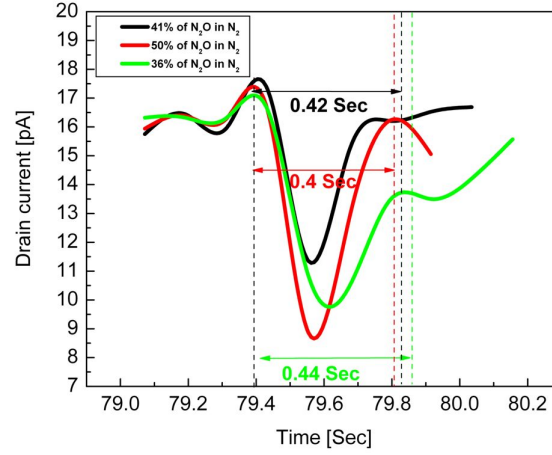


**Figure 5.28:** Response of SET to the injection of the mixture of gases into the flow cell.

gate terminal increase, thus providing further increase in the charge, creating an electrostatic state which lies in the stable Coulomb diamond region, which will not allow any increase in the drain current. With the removal of gas from the flow cell, the charge on the gate terminal is again modified so that an increase in drain current is electrostatically favorable.

The concentration of  $N_2O$  gas was 41% in  $N_2$  for Figure 5.28. The change in the drain current was observed because of the incorporation and removal of the  $N_2O$  gas from the flow cell. It can be observed that the change in the drain current is an order of magnitude different when the gas is introduced into the flow cell and also when the gas is removed from the flow cell.

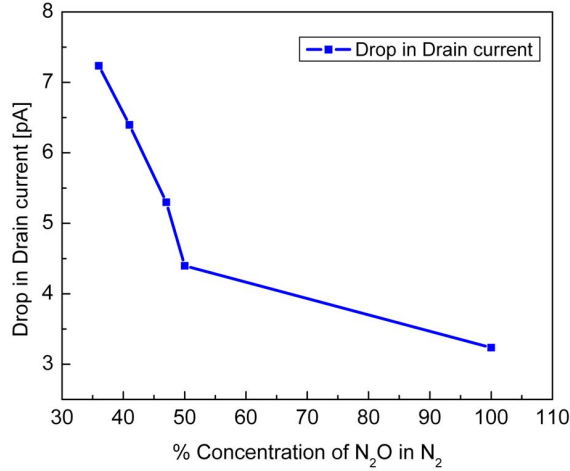
The  $N_2O$  concentration is 41% in  $N_2$ . The lowest concentration of the  $N_2O$  gas that was detected in this configuration was 36 percent of  $N_2O$  in  $N_2$ . Changing



**Figure 5.29:** Variation in the drain current drop and the relaxation time of the SET corresponding to different concentrations of the injected gas.

the concentration of  $N_2O$  gas in the mixture resulted in a near-linear modulation in the magnitude of the drain current. For a concentration of 36% of  $N_2O$  gas in  $N_2$ , it was found that the drain current decreases by 7.235 pA. For a concentration of 41% of  $N_2O$  gas, it was found that the drain current decreases by 6.396 pA. For a concentration of 50 % of  $N_2O$  gas in the mixture, it was found that the drain current decreases by 4.397 pA. The relaxation times for different concentrations of the  $N_2O$  gas was demonstrated to vary as well. As the concentration of the gas increase the relaxation time decreases, as shown in Figure 5.29. It is then possible to distinguish between different concentrations of the gas based on the magnitude drop in the drain current and also difference in the relaxation times.

The reduction in the drain current of the SET device decreases with the increase in the concentration of  $N_2O$  gas. For lower concentrations of the sensing species the

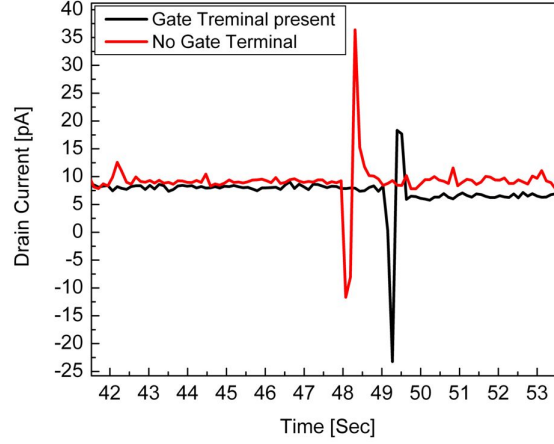


**Figure 5.30:** The SET gas sensor is very sensitive at lower concentrations of  $N_2O$ .

SET device is more sensitive and for higher concentrations the sensitivity of the SET sensor decreases, as shown in Figure 5.30.

The gas molecules adsorbed on to the gate terminal of the SET device create extra charge proportional to the number of gas molecules adsorbed modulating the tunneling properties. Thus, the SET device is acting as an electrometer. To confirm this sensing behavior, a SET without any gate terminal was fabricated. It was observed that with out the gate terminal the drop in the drain current reduced by 40%. Figure 5.31. shows the variation in the drain current for the device having the gate terminal as the sensing element and for the device without the gate terminal present.

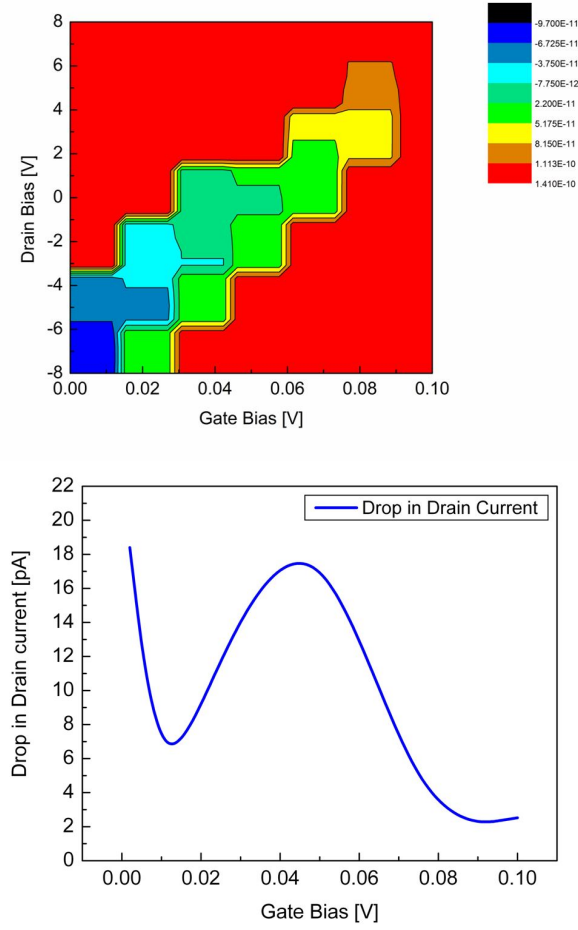
The presence of the gate electrode which is used as a sensing element is found to enhance the sensing ability of the SET device. SET device with out the gate electrode was found to be sensitive to gas sensing, due to the charge accumulation resulting



**Figure 5.31:** The SET response with the gas injection for devices with and without the gate terminal.

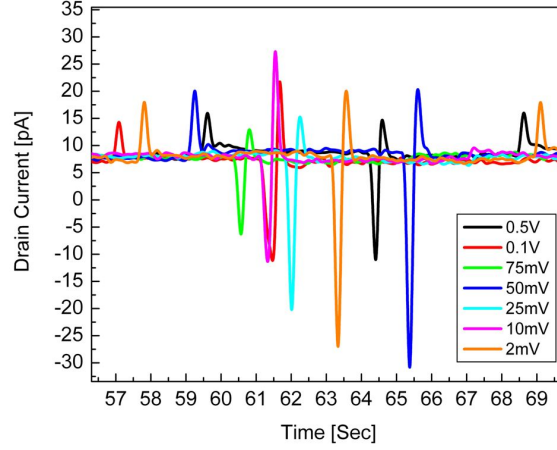
from the gas adsorption onto the activating  $Al_2O_3$  oxide, acting as a secondary gate terminal. The sensitivity of the sensor can be modulated by the presence of the gate electrode as the sensing element.

The biasing of the gate electrode provides a fixed charge on the gate electrode. The adsorption of the gas molecules on the gate terminal will increase the charge on the gate terminal. The tuning of the SET characteristics can be achieved by fixing the gate bias and changing the amount of gas species introduced into the sensing chamber. Figure 5.32(a) shows the effect of variation of the gate bias with the variation of the source drain bias on the drain current of the SET device. The Coulomb diamonds show the electrostatically stable regions where there is no increase in the current, until the blockade voltage is overcome [89]. The application of a particular bias on the gate terminal will fix the voltage in the Coulomb diamond regions, and the introduction



**Figure 5.32:** (a) Coulomb diamond regions showing the drain current variation with the change in gate bias, (b) Oscillating drain current with change in gate bias is in correlation with the Coulomb diamonds shown in (a).

of the gas species will increase the charge on the gate, thus shifting the bias point to a different location on the Coulomb diamonds. This shifting of the gate bias point will allow for the tuning of the sensitivity of the device, resulting in the drain current variation. Figure 5.32(b) clearly shows the variation in the drain current drop as the gate bias is changed. The oscillatory nature of the change in the drain current



**Figure 5.33:** SET response to gas injection for different gate biases.

reduction is in accordance with the Coulomb diamonds. The SET device shows the variation in the drain current reduction with the introduction of the gas species, with different gate bias applied, which is clearly shown in Figure 5.33.

A novel gas sensor based on the room temperature operating single electron transistor is demonstrated [90]. The SET gas sensor is used to detect  $N_2O$  gas. The incorporation of  $N_2O$  gas resulted in the change of the device characteristics of the SET device, the reduction in the blockade voltage is observed, an appreciable reduction in the drain current of the SET device by an order of magnitude. The SET gas sensor shows the relaxation time of 400 ms for a concentration of 36% of  $N_2O$  gas in  $N_2$ . The reduction in the drain current of the SET device decreases with the increasing concentrations of  $N_2O$  gas. The sensitivity of the SET gas sensor is higher for lower concentrations. The device sensitivity can be tuned by controlling the gate potential.

# Chapter 6

## Conclusion

### 6.1 Contributions:

The research undertaken during this dissertation has led to significant progress in the development of technologies for the room temperature operating single electron transistors, fabricated using focused ion beam technologies. The research also explored the model development of a multi dot SET system. The fabricated SET device is used as a gas sensor. The major contributions of this work are summarized below.

† The capabilities of FIB etching and deposition for the device fabrication have been understood.

† The research has showed that FIB etching technologies for device fabrication have limitations for the fabrication of conducting nano islands below 40nm due

to the beam interaction.

† The FIB deposition technologies have been successfully utilized for the fabrication of conducting nano islands in tungsten, having an average diameter of 8nm. This technique can be applied to the fabrication of sub 10nm nano islands in any material, using FIB deposition.

† First demonstration of FIB deposition based technique, for fabrication of sub 10 nm nano islands.

† The FIB deposition technologies have been successfully applied for the realization of room temperature operating single electron transistors.

† First demonstration of room temperature operating single electron transistor using FIB deposition. The SET devices fabricated using FIB deposition have the charging of 160.0 meV, with the total capacitance of 0.5 aF, and the tunnel resistance of few tens of GΩ.

† The pre island fabricated devices have larger capacitance than the post island fabricated devices. The coulomb blockade length of the pre island fabricated device was smaller than that of the post island fabricated devices.

† Different device configurations reducing the device capacitance have been studied. The reduction in the dimensions of the connecting nano electrodes, would reduce the total capacitance of the device and, hence would improve the charging energy of the device.



† The effect of the tunnel junction resistance and the thickness of the tunneling oxide on the device characteristics is understood.

† Device model for the multidot SET system using soliton model was found to describe the device characteristics of the fabricated device.

† First room temperature operating SET device, used as a gas sensor.

## 6.2 Future work

The present work demonstrates the technology necessary for the fabrication of room temperature operating single electron transistors, using focused ion beam technologies. In order to control the blockade length of the fabricated device, the number of nano islands participating in conduction should be minimized. Continuing efforts are needed for the realization of single dot SET system. To achieve the single dot SET system, understanding of FIB beam dynamics, and the beam properties, should be understood.

The soliton-based device model can be improved and continued effort is needed in the modeling of the device behavior. In particular the model can be improved by incorporating the inter-island capacitance effects and the asymmetry in the tunnel junction properties of the junctions. The dimensions of the deposited nano-islands are  $\sim 8\text{nm}$  with the variation of  $\pm 1\text{nm}$ , the spacing between the nano-islands is

$\sim 4\text{nm}$ . The deposited nano-islands follow the Gaussian distribution. The inter-island capacitance and the tunnel junction resistances could be included in the device modeling. In order to fully understand the device behavior, a quantum mechanical model exploring the tunneling events between the islands and their neighbors, should be investigated.

For the SET devices to be useful for practical applications, arrays of these device should be fabricated. Technologies necessary for the realization of multiple SET devices should be explored. The SET devices being sensitive electrometers, can be integrated as front end of the sensing system. The demonstrated gas sensing application could be investigated further to explore to sense different gases. This concept can be applied to many different sensors using SET devices. Room temperature operating single electron transistors have a great potential to be integrated into many applications.

# Chapter 7

## Appendix

### 7.1 FIB etching recipe

Deposition of  $Al_2O_3$ :

**Table 7.1:** Deposition Process parameters

Deposition material	$Al_2O_3$	Ni
RF Power	900 W	650W
DC Bias	-451 V	-463 V
Substrate bias	0	0
Process pressure	9.6 m Torr	5.7 m Torr
Gas flow	Ar: 14.0 SCCM, $O_2$ : 2.0 SCCM	Ar: 7.0 SCCM
Substrate temperature	25 C	25 C
Deposition time	30 minutes	30 minutes

Process parameters for the fabrication of SET structures using FIB etching:

**Table 7.2:** FIB process parameters for micro and nano-scaled etching

	Micro scaled electrodes	Nano scaled leads
Beam	MI-300	MO-50
Beam current	4.0 - 8.0 nA	20.0 - 58.0 pA
Dwell time	128 $\mu sec$	128 $\mu sec$
Frame number	50	10
Magnification	256 $\mu m \times 2$	32 $\mu m \times 2$
Etch time	6 minutes	5.3 minutes

Beam MO-20 is used to pattern the structure with out the island. Table1: Processing parameters Figure

Beam :(MO-20) Centre-Centre distance: 5.3Å Line spacing : 5.3Å Dwell time : 0.4  $\mu sec$  Magnification : 145K Number of repetitions: 5

## 7.2 FIB Deposition Recipe

Deposition of Tungsten using FIB deposition:

### 7.2.1 Nano island deposition recipe:

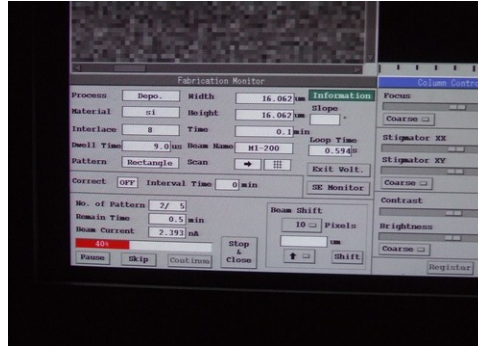
Deposition of Tungsten nano islands:

The process parameters for the nano-island fabrication are shown in the Table 7.3.

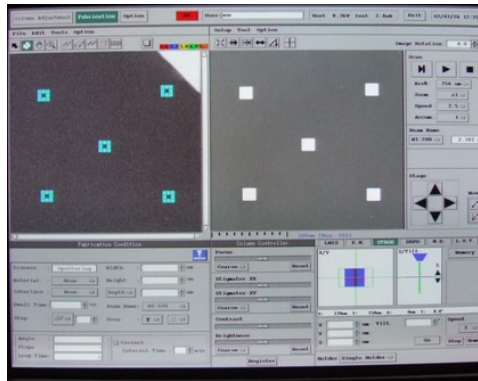
The FIB snap shot for the fabricated nano islands are shown in the Figure 7.1 and Figure 7.2.

**Table 7.3:** Process parameters for FIB Deposition of nano islands

Deposition parameters:	[Dimensions $16.062 \mu\text{m} \times 16.062 \mu\text{m}$ ]
Interlace	8
Dwell time	$9.0 \mu\text{sec}$
Total time	0.1 minutes
Beam	MI-200
Loop time	0.594 sec(decided by the software)
Beam current	2.334nA



**Figure 7.1:** process parameters for the nano-island fabrication



**Figure 7.2:** Snap shot of the fabrication window on FIB system for the nano islands.

## 7.2.2 Connecting nano leads deposition recipe:

Deposition of the leads:

**Table 7.4:** Process parameters for FIB Deposition of nano-scaled connecting leads

Deposition parameters:	[Lead dimensions: $55\ \mu\text{m} \times 5\ \mu\text{m}$ ]
Interlace	2
Dwell time	$0.5\ \mu\text{sec}$
Total time	2.0 minutes
Beam	Beam -01
Loop time	0.035 sec(decided by the software)
Beam current	0.116nA

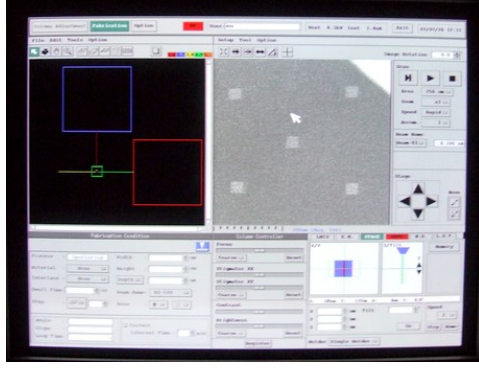
### 7.2.3 Deposition of probing pads recipe:

Deposition of pads:

**Table 7.5:** FIB Deposition Process parameters

Deposition parameters:	[Pad dimensions $100\ \mu\text{m} \times 100\ \mu\text{m}$ ]
Interlace	2
Dwell time	$0.5\ \mu\text{sec}$
Total time	10minutes
Beam	Beam -01
Loop time	1.280 sec(decided by the software)
Beam current	0.116nA

The FIB snap shot for the probing pads shown in the Figure 7.3.



**Figure 7.3:** Snap shot of the fabrication window on FIB system for the probing pads.

## 7.3 MATLAB Code for computing the device characteristics of multi dot SET

This code is for a multi dot SET with device configuration DT2:

The original code for the I-V characteristics for a single dot SET system is taken from reference [52], the original code is modified for the multi dot SET system by incorporating the Soliton model.

```
k=1.380662e-23;
```

```
T=300.0; e=1.602e-19; C1=0.9854e-19; C2=0.9854e-18; Cg=0.38e-18;
```

```
Csum=sqrt(Cg*Cg+4*(C1)*Cg);
```

```
num=input('newlineNumberofislandsnewline');
```

```
Ec = (e^2)/(2 * Csum); R1=29.2e9; R2=50.13e9; V=[-10000:10000]; V=V*600e-6;
```

```
V=V+eps; N=[-8:8]; n=length(N); Nt=N'*ones(size(V)); Vt=ones(size(N))'*V;
```

Inew=0; Inew1=0;

for Vg=-0.01:-0.04:-0.09 for i=1:num

Deisling model

$V1 = (e * (Vt + Vg) / Csum) * \exp(-i * (\cosh(1 + (Cg / (2 * (C1 + C2))))))$ ;  $+(Vg * (Cg / (Csum)))$ ;

$V2 = (e * (Vt - Vg) / Csum) * \exp(-(i + 1) * \cosh(1 + (Cg / (2 * (C1 + C2))))))$ ;  $-(Vg * (Cg / (Csum)))$ ;

$p1 = 1 / (e^2 * R1)$ ;  $p2 = 1 / (e^2 * R2)$ ;

$DEr1 = (V1 * e) - Ec$ ;  $DEl1 = (-V1 * e) - Ec$ ;  $DEr2 = (V2 * e) - Ec$ ;  $DEl2 = (-V2 * e) - Ec$ ;

$r1 = p1 * DEr1 / (1 - \exp(-DEr1 / (k * T)))$ ;

$l1 = p1 * DEl1 / (1 - \exp(-DEl1 / (k * T)))$ ;  $l2 = p2 * DEl2 / (1 - \exp(-DEl2 / (k * T)))$ ;

$r2 = p2 * DEr2 / (1 - \exp(-DEr2 / (k * T)))$ ;

$x = r1 + l2$ ;  $y = l1 + r2$ ;  $prodxl = x$ ;  $prodyu = y$ ;  $prodxl(1, :) = \text{ones}(\text{size}(V))$ ;  $prodyu(n, :$

$) = \text{ones}(\text{size}(V))$ ;  $\text{for } i = 1 : n - 1, \text{prodxl}(i + 1, :) = \text{prodxl}(i, :) * x(i, :)$ ;  $prodyu(n - i, :$

$) = \text{prodyu}(n - i + 1, :) * y(n - i + 1, :)$ ;  $\text{endro} = \text{prodxl} * \text{prodyu}$ ;  $\text{sro} = \text{sum}(\text{ro})$ ;  $\text{for } i =$

$1 : \text{length}(V), \text{ro}(:, i) = \text{ro}(:, i) / \text{sro}(i)$ ;  $\text{endI} = -e * \text{sum}(((l2 - r2) * \text{ro}))$ ;

$\text{Inew1} = (\text{Inew1}) + \text{I}$ ;  $\text{endInew} = \text{Inew1}$ ;  $\text{plot}(V, \text{Inew}, 'r') \text{hold on}$ ;

$\text{xlabel}(' \text{Drain voltage}[V]')$ ;  $\text{ylabel}(' \text{Drain current}[A]')$ ;  $\text{title}(' \text{DT2 Post island fabricated device}')$ ;

end



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- 2) Figure 3. (a) Schematic cross section and (b) top view of the first reported Si SET, which was fabricated using double-gate MOS structures. (c) Measured conductance as a function of the gate voltage. The CB oscillation was observed at 400 mK. Reprinted with permission from [10]. Copyright 1989 by the American Physical Society.
- 3) Figure 8. (a) Schematic view of the Si pattern used for SET fabrication by V-PADOX [25] (b) Cross-sectional TEM image of the thin Si region.
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- 5) Figure 11. (a) A schematic of the SET using Si nanocrystals. (b) Drain current contour plot in the gate voltage and drain voltage plane at 20 K. White-coloured CB regions designate current  $<10$  pA. Reprinted with permission from [47]. Copyright 2000 Japan Society of Applied Physics.

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2. Figure 4. A schematic sketch of a vertical quantum dot. A narrow pillar is defined out of a heterostructure where two barriers are formed by layers of AlGaAs. The QD is formed between the layers and electrons can tunnel into and out of the dot. The barriers need not be of the same thickness. Measurements of conductance or capacitance on such structures are described in the text.

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