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DEVELOPMENT AND VERIFICATION OF AUTOMATED FIXTURES FOR FUNCTIONAL TESTING OF SPACE GRADE PRINTED CIRCUIT BOARD ASSEMBLIES

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DEVELOPMENT AND VERIFICATION OF AUTOMATED FIXTURES FOR FUNCTIONAL TESTING OF SPACE GRADE PRINTED CIRCUIT BOARD ASSEMBLIES

By

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A REPORT

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List of Abbreviations

AC – Alternating Current
ANSI – American National Standards Institute
AOI – Automated Optical Inspection
BOM – Bill of Materials
CAD – Computer Aided Design
COTS – Consumer off the Shelf
DAQ – Data Acquisition and Control
DC – Direct Current
ECAD – Electrical CAD
ESD – Electrostatic Discharge
FMEA – Failure Mode & Effects Analysis
HET – Hall-effect Thruster
IC – Integrated Circuit
IPC – Institute of Printed Circuits
LPF – Low Pass Filter
PCB – Printed Circuit Board
PCBA – PCB Assembly
PMA – Propellent Management Assembly
RMS – Root Mean Square
SMT – Surface Mount Technology
SPICE – Simulation Program with Integrated Circuit Emphasis
TH – Though Hole
UUT – Unit Under Test
VI – Virtual Instrument

Abstract

Orbion Space Technology is a developer and manufacturer of electric propulsion systems for military and commercial spacecraft. Orbion's products include a Power Processing Unit (PPU) which is utilized for power and control of the satellite propulsion system. These PPUs are complex electro-mechanical assemblies that include multiple Printed Circuit Board Assemblies (PCBA) and are built to IPC standards. To ensure smooth fabrication and to reduce the risk of complications from in-process rework of PCBAs, comprehensive electrical functional testing at the board-level is required before higher-level assembly. Electrical functional testing provides verification of quality, workmanship, and manufacturing defects of the PCBAs. The test fixtures detailed in this report are intended for use in a manufacturing line and are rugged, technician-friendly, and capable of meeting Orbion's testing requirements. This project delivers a functional 200V power supply, a functional automated test fixture, and a design for a second automated test fixture.

1 Introduction

1.1 Project Overview

The first idea for an electric ion thruster propulsion system was introduced in 1911, with the first being flown in space in NASA's SERT-1 mission in 1964 [1]. Since then, electric propulsion systems have been used for many satellite missions in low earth orbit, geosynchronous orbit, as well as deep space [2]. In the modern space age, electric propulsion systems are used to support the ever-growing constellations of satellites, such as SpaceX's Starlink, and even for scientific discovery missions elsewhere in our solar system, such as NASA's Psyche mission [3].

Electric propulsion is a desirable technology for these types of space missions because of the high specific impulse and high fuel efficiency of electric propulsion systems when compared to their chemical or cold gas counterparts [4]. While chemical thrusters have a very large mass flow rate of their propellant and can rapidly accelerate a satellite, chemical thrusters are not practical for long term missions due to their relatively lower exhaust velocity. The very high exhaust velocity of the electric thruster and lower mass flow rate allows for a much longer lasting propellant supply and mission lifetime.

Orbion Space Technology's electric propulsion system, the Aurora, is a Hall-Effect Thruster (HET) System [5], shown in Figure 1.1. Each Aurora HET System is composed of three key components: the Hall-Effect Thruster itself, the Propellant Management Assembly (PMA), and the Power Processing Unit (PPU). The PMA controls the flow of gas to the HET, while the PPU supplies power and commands the entire system.

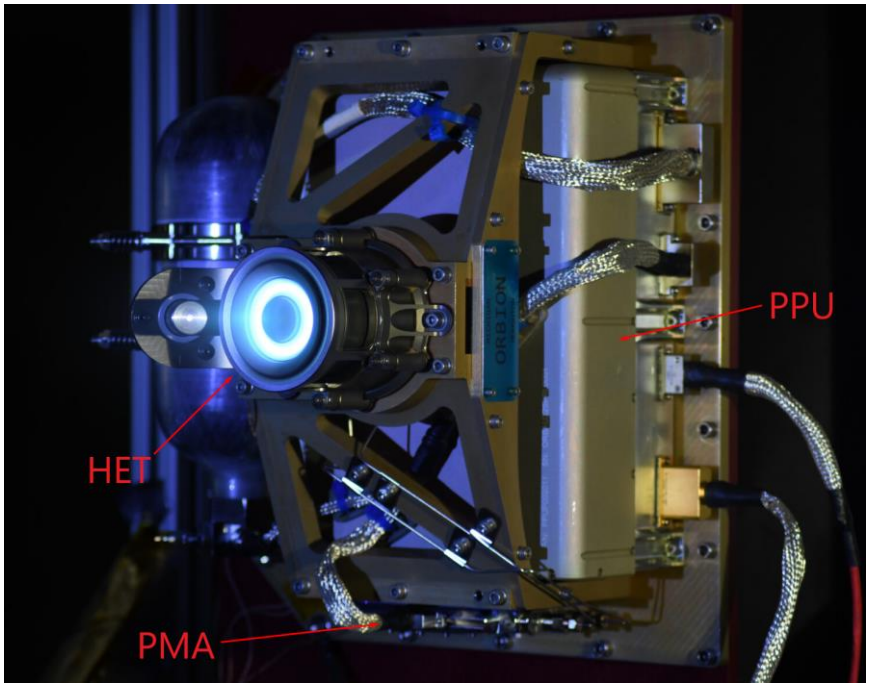

Figure 1.1. The Aurora Hall-Effect Thruster System.

The PPU is a very complex electro-mechanical assembly overseeing the control of the PMA and HET. The PPU manages gas flow, regulates output power, controls thruster ignition, and employs feedback loops to constantly monitor and adjust the outputs via a control algorithm.

To perform these complex tasks, the PPU features a myriad of Printed Circuit Board Assemblies (PCBAs), each performing a unique role in thruster operation. Several circuits inside of the PPU are single points of failure for the device. That is, if one of the circuits on a PCBA breaks, there is no alternative action for continuing to operate the thruster. As such, the PPU must be tested thoroughly for the extreme environment of space in order to ensure the operation of the Aurora HET system for several years or even decades with no failures.

Shown in Figure 1.2 is a simplified assembly flowchart of the PPU. Electrical and mechanical parts are first assembled into each bare PCB via surface mount and through hole technology, then each PCBA is assembled into the PPU top assembly with additional mechanical parts. While only two examples of PCBAs are shown in this diagram, there are several other unique PCBAs in the design.

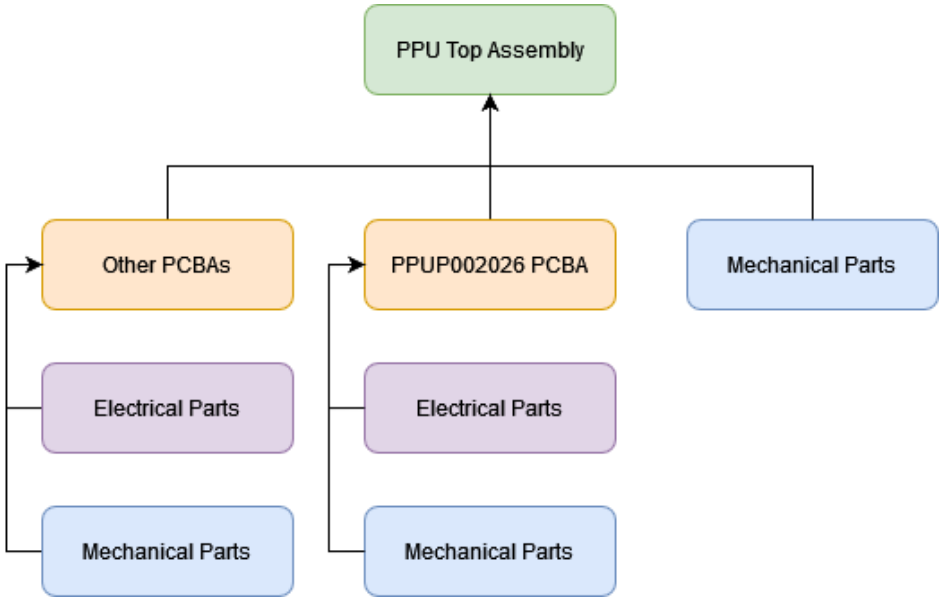

Figure 1.2. Simplified assembly flowchart for the Aurora PPU.

To achieve the high reliability standards required of the Aurora HET system, each PCBA in the PPU is manufactured and screened by automated optical inspection, automated x-ray inspection, and visual inspection before being assembled into a complete PPU. While these visual inspection methods are effective at finding potential anomalies in the soldering and placement of components, there is no guarantee that each PCBA will function as designed. The best and most cost-effective method determined by Orbion to verify the functionality of the PCBAs is to perform board-level electrical functional tests.

Board-level functional testing is a method to verify the quality, workmanship, and manufacturing of the PCBAs by operating them in a flight-like manner. Performing functional tests at the board-level prevents potential defects from reaching a higher-level assembly and collects data about each unit for better unit traceability and failure analysis.

A method for performing an electrical functional test is to make a separate PCBA with test circuits on it, and a “bed of nails” out of spring-loaded metal contacts that electrically interface with the Unit Under Test (UUT). This way, electrical signals to and from the test circuits can be passed between the UUT and the fixture. Creating each test fixture will require definition of requirements, designing the PCBA and associated hardware, manufacturing each component, and then verifying the functionality of the entire fixture. The objective of this project is to provide verified test fixtures for electrically testing PPU PCBAs in a cost effective and flight-like manner, to increase total testing coverage before a full box-level PPU integration.

1.2 Organization

First, the project requirements will be listed and discussed in the context of this project in Chapter 2. Understanding the requirements for the designs is a key first step before determining the methods employed for designing around the requirements. Chapter 3 discusses the methods for design and verification of the DC-DC converter and test fixtures.

Chapter 4 details the design and verification effort for the 200V Isolated DC-DC Flyback Converter. The PPUP002026 Test Fixture is designed and verified in Chapter 5, utilizing the 200V Converter from Chapter 4. Lastly, the Backbone Test Fixture design for testing the PPUP002046, PPUP002048, and PPUP002085 is covered in Chapter 6.

2 Project Requirements

2.1 Introduction

The project requirements for the designs of the 200V power supply and the test fixtures are defined and detailed below. The first stage in any engineering design is to determine and list all requirements for the design. Listing all requirements clarifies what exact specifications are required to be developed into the designs. Project outcomes are measured by the project requirements being executed during the design and verification phases. Project requirements guide the project in a clear and measurable direction. The project requirements chapter will outline the general requirements for Orbion electro-mechanical designs, the specific requirements for the testing and fixturing of PCBAs, as well as the requirements for the DC-DC converter. Understanding the project requirements is a crucial preliminary step before determining the methods and details to be employed in any engineering design.

2.2 General Standards and Reliability

The general requirements used at Orbion for new designs are listed and explained in the context of this project below. The requirements are crucial for the long-term functionality and reliability of the test fixtures and DC-DC converter, as these designs are planned to be adapted into a manufacturing environment, where robustness and reliability are key.

Design shall conform to Class 2 of the following standards: IPC-2222B, IPC-6012E, IPC-J-STD-001H, IPC/WHMA-A-620E.

The IPC standards listed in this requirement are internationally recognized standards in the electronics industry. IPC classifies electronics designed to these standards as classes 1, 2, and 3. The fixtures developed in this project will be defined as class 2 electronics. Class 2 is defined as: products where continued performance and extended life is required, and for which uninterrupted service is desired, but not critical [6]–[9].

IPC-2222 is the Sectional Design Standard for Rigid Organic Printed Boards [6], defining the specific requirements for designing quality rigid circuit boards. IPC-6012 is the Qualification and Performance Specification for Rigid Printed Circuit Boards [7], detailing requirements revolving around plating and other physical features. IPC-J-STD-001 is the standard for soldered electrical and electronic assemblies [8], covering everything about the assembly of a PCB and its parts. IPC/WHMA-A-620 is the standard for electrical wiring harness assemblies [9], covering everything about connectors, wires, labels, and more. While there is not a standard for the specific design of a wiring harness as there is for PCBs, IPC/WHMA-A-620 outlines good and bad practices to apply to design.

Following IPC standards to the Class 2 requirements will ensure the general reliability of the Test Fixture, as it will need to operate for many years of production cycles.

Design shall be Hi-Pot tested to at least 250V.

High Potential, or Hi-Pot testing, is a method used to verify no electrical shorts are present and no insulation material is damaged after manufacturing a harness [9] or PCB [10]. Hi-pot testing ensures the electrical insulation provided by the non-conductive PCB layers and wire insulation is sufficient to isolate high voltages. In the case of a PCB, the Hi-Pot testing is performed by the third-party manufacturer between the power and ground planes. The wiring harness Hi-Pot testing is performed at Orbion between all wires.

Design shall reference all mounting holes to CHASSIS/Earth Ground.

CHASSIS is a net in the PCB that is typically referenced to earth ground. The PCBs designed in the project all have mounting holes, so standoffs can be attached, or so they can be mounted to an enclosure or other. Any electrical connection that may come in contact with the lab bench needs to be CHASSIS. This requirement is standard practice at Orbion and is important to keep everything consistent. In some setups it is critical that GND and CHASSIS are not directly connected.

Design shall utilize automotive-grade electrical parts or equivalent reliability/quality when possible.

Automotive parts are tested to higher standards and are made for high-reliability environments when compared to Consumer off the Shelf (COTS) parts [11]. Using automotive grade parts will guarantee the designs in this project will not unexpectedly break in their lifetime of usage, as automotive-grade components are extensively tested, over large temperature ranges and for a long lifetime.

While automotive parts are acceptable for the PCBAs contained in this project, the PPU PCBAs tested by the test fixtures utilize some components tested to Military Standards (MIL-STD), which are more extensively tested for the environment of space.

2.3 200V Isolated DC-DC Flyback Converter

The specific requirements for the 200V Converter are listed and explained below. The requirements are crucial for the electrical functionality and reliability of the power supply. The power supply is utilized in the PPUP002026 Test Fixture for powering the Unit Under Test (UUT).

Design shall deliver 200V ±10V DC, <10Vpp ripple, and >10mA on the output.

This requirement specifies the output voltage and current of the converter. It must deliver a 200V signal, with a magnitude between 190V and 210V, a voltage ripple no greater than 10V from peak to peak, and a current output of at least 10mA. This specification states the input power requirements of the PPUP002026, so if the 200V converter can deliver power to this specification, the PPUP002026 will operate correctly.

Design shall have an input voltage range of 12-24V.

There is most commonly a 12V or 24V power supply connected to a fixture or development PCBA at Orbion, so being able to operate in this voltage range is a requirement. As the topology of the converter is not specified in the requirements, there is no input current requirement. Also, because the 200V converter is for development and testing purposes, supplying extra input power is not a concern.

Shall be designed to electrically and mechanically interface to another PCBA as a "Daughterboard."

This requirement states that the converter will essentially be rigid mounted to another PCBA, making the converter part of that assembly. Not necessarily soldered, but not designed to be removed often. By designing this converter as its own PCBA, the converter can be used easily in future projects. In the context of this project, it allows for easily replacing the converter if it were to fail, or if an updated version was developed with better characteristics.

Shall have output protections to protect downstream devices.

Overvoltage protection is necessary to prevent devices connected to the output of the converter from being damaged if something were to fail in the converter. In the context of this project, it is related to ensuring the Electrical Interface for the PPUP002026 will not damage the UUT by overvolting the power rail of the UUT.

2.4 Test Fixture Requirements

In this section, the requirements specific to the test fixtures designed in this project are listed and explained. The operational purpose of the test fixtures is to functionally test the UUT. Many of the requirements revolve around the safety of the fixture and the UUT. The requirements are put in place to lower the risk of component damage during operation of the fixtures. Other requirements detail the interfaces for the test fixtures and the operation of the test fixtures.

Fixture shall implement a Data Acquisition and Control (DAQ) system.

A DAQ system is necessary for exactly what it stands for - acquiring data and controlling the overall fixture. The DAQs are needed to make this test automated. Without the DAQs, there is no interface between the software and the PCBA to acquire data or control the fixtures. This project utilizes DAQs to record test data as well as control the fixture during the automated testing.

Fixture shall provide a method of enabling and disabling all power sources which are connected to the UUT, via an external interface.

This requirement is in place so that the DAQ system will be able to disable all power to the UUT for safety of the UUT, the fixture, and the operator. The UUT must not be

connected to any power source while being installed or removed from the fixture. This requirement allows for the UUT to be mated and de-mated with the fixture without completely unplugging the 24V power supply from the fixture.

Fixture shall implement a “Zap-Trap.”

A “Zap-Trap” consists of two diodes with opposing polarity, a capacitor, and a resistor, all in parallel and connected between CHASSIS and GND. These four components will ensure that any voltage applied to the PCB through the CHASSIS or GND nets will be dissipated to protect the UUT and fixture from ESD events. ESD events can be harmful to any electronics as they are typically thousands of volts in magnitude, so having means in place to suppress the ESD events is crucial.

Fixture shall be classified as a ESD Sensitive Device, Human Body Model 1A, per ANSI/ESD S20.20-2021.

Like IPC, ANSI standards are widely used across the industry. ANSI/ESD S20.20-2021 is the standard for Protection of Electrical and Electronic Parts, Assemblies and Equipment [12]. This standard covers protection methods for electrical parts. By classifying the fixtures as ESD sensitive devices, they must be handled with care, only in ESD-safe environments. They need to be classified as such to guarantee the safety of the fixtures and to ensure their long service life.

Fixture shall function off of a single external 24V barrel jack power supply (excluding DAQ system).

This requirement is for simplicity; using a single 24V power supply allows for the fixture to only have one power interface and then regulate that 24V to any other voltages that the fixture may need. The requirement specified a barrel jack, so any 24V supply with a standard connection will work. With all the power conversion contained to the PCBA, the number of external components needed to operate the fixture is reduced.

DAQs are excluded from this requirement, as many standalone DAQ systems are powered via a USB port or their own adapter, therefore the DAQs do not need to be powered by the fixture PCBA.

Fixture shall enable automated testing with a total test time of 15 minutes or less.

That is, the total time to install the UUT, execute the automated test, and remove the UUT shall be less than 15 minutes. This requirement is key in order to not slow down the manufacturing line.

2.4.1 PPUP002026 Test Fixture

The specific requirements for the PPUP002026 Test Fixture are listed and explained below. The requirements are crucial for the electrical functionality and reliability of the

test fixture. Many of the requirements revolve around the safety of the fixture and the UUT. Other requirements detail the specific pass/fail criteria for the UUT.

Fixture shall mechanically interface with the UUT per the PPUP002026 Assembly Drawing, without damaging the UUT.

This requirement referenced the PPUP002026 PCB Assembly drawing, which characterizes the profile of the PPUP002026 PCBA. Mounting hole size and locations are present, as well as bounding boxes for components. Following the details of this drawing is imperative to design a proper mounting mechanism that will not damage the UUT.

Fixture shall electrically interface with the UUT per the PPUP002026 Assembly Drawing, without damaging the UUT.

In a similar fashion to the mechanical interface, the assembly drawing describes where all of the electrical interfaces are, and their maximum ratings. The fixture shall not exceed any maximum ratings set by the assembly drawings. Following the details of this drawing is imperative to design a proper electrical interface that will not damage the UUT.

Fixture shall verify all three amplifier circuits of the PPUP002026 operate as designed within acceptable limits for a DC input.

This requirement specifies the functional test requirement of the PPUP002026. The fixture shall drive the input of all three cascode amplifiers with a 0-3.3V control signal and verify the output is compliant to the transfer function from the PPUP002026 assembly drawing. By measuring the three amplifier circuits and comparing them to transfer function defined pass/fail criteria, the fixture can automatically determine if the UUT is operating as designed. In this project, the software operating the PPUP002026 Test Fixture will compare these measurements and determine the result, with and without representative flight termination RC loads.

Further details of the design of the PPUP002026 are omitted for confidentiality.

Fixture shall implement representative electrical loads of the outputs of the PPUP002026, with the ability to enable or disable these loads via external interface.

It is important to test both with and without electrical loads connected. Without the loads is important because it verifies the basic functionality without introducing a dangerous amount of energy into the system initially in case there is a failure. With loads it is important because loading the outputs stresses the system in a “flight-like” manner and can potentially find issues hidden otherwise. The fixture shall implement representative flight termination RC loads for the cascode amplifier outputs.

In this project, the loads need to be controlled via the DAQ, so that the test software can automatically enable or disable the loads, for different parts of the test.

2.4.2 Backbone Test Fixture

The specific requirements for the Backbone Test Fixture are listed and explained below. The requirements are crucial for the electrical functionality and reliability of the test fixture. Many of the requirements revolve around the safety of the fixture and the UUT. Other requirements detail the specific pass/fail criteria for the UUT.

Fixture shall mechanically interface with the UUTs per the PPUP002046, PPUP002048, and PPUP002085 Assembly Drawings, without damaging the UUTs.

This requirement referenced the PPUP002046, PPUP002048, and PPUP002085 PCB Assembly drawings, which characterize the profile of the PPUP002046, PPUP002048, and PPUP002085 PCBAs. Mounting hole size and locations are present, as well as bounding boxes for components. Following the details of these drawings is imperative to design proper mounting mechanisms that will not damage the UUTs.

Fixture shall electrically interface with the UUTs per the PPUP002046, PPUP002048, and PPUP002085 Assembly Drawings, without damaging the UUTs.

In a similar fashion to the mechanical interface, the assembly drawings describe where all of the electrical interfaces are, and their maximum ratings. The fixture shall not exceed any maximum ratings set by the assembly drawings. Following the details of these drawings is imperative to design proper electrical interfaces that will not damage the UUTs.

Fixture shall verify all MOSFETs, diodes, and ICs present on the PPUP002046, PPUP002048, and PPUP002085 PCBAs operate as designed by electrically loading the circuits in a “flight-like” manner.

This requirement specifies the functional testing requirements of the PPUP002046, PPUP002048, and PPUP002085. For all three PCBAs, the fixture shall verify all parts are populated with correct polarity and value (or manufacturer part number) per the released PCBA drawing. This is a byproduct of the functional testing, as the tests will fail if components are installed incorrectly.

For the PPUP002046, the fixture shall drive the gates of several MOSFETs with a 15V ±3V gate drive signal with a frequency range of 30kHz to 100kHz with a 50% to 90% duty cycle and observe acceptable operation MOSFETs per the manufacturer datasheet. The fixture shall also verify the phase 1 and 2 main drive snubber circuits properly clamp expected flyback voltages per the manufacturer datasheets.

For the PPUP002048, the fixture shall drive the gates of several MOSFETS with a 15V ±3V gate drive signal with a frequency range of 30kHz to 100kHz with a 50% to 90% duty cycle and observe acceptable operation MOSFETs per the manufacturer datasheet.

For the PPUP002085, the fixture shall drive the input channels of two ICs with a 15V ±3V gate drive signal with a frequency range of 30kHz to 100kHz with a 50% to 90%

duty cycle and observe acceptable operation of the outputs of the ICs per the manufacture datasheet.

Further details of the designs of the PPUP002046, PPUP002048, and PPUP002085 are omitted for confidentiality.

2.5 Conclusion

The project requirements detailed above establish the exact specifications that are required to be developed into the designs in this project. Understanding the project requirements is an important step in determining the methods and details to be employed in any engineering design. The methods of designing for these requirements will be described in the next chapter.

3 Methods

3.1 Introduction

The methods chapter establishes the various tools and design conventions used for development of the test fixtures and DC-DC converter. The design tools are software packages that aid in the design of circuits, schematics, and layout, as well as new software code. The design conventions are for drawing schematics, selecting electrical parts, laying out the PCB, writing code, and reviewing the developed designs. The manufacturing process details the process and standards for building physical hardware. The verification tools include equipment used to test the manufactured hardware. Verification methods detail how the tools are used for PCBA and software evaluation.

3.2 Design

3.2.1 Design Tools

Altium Designer

Altium Designer is a leading ECAD tool, focusing on the creation of electrical schematics and PCB layouts [13]. Altium includes many features common in PCB-oriented ECAD tools: schematic capture, PCB layout, BOM management, and more. Several of these features were utilized in this project.

Additionally, Altium features a component library function. This feature facilitates the creation of schematic “symbols” and PCB “footprints.” These symbols and footprints represent a connector, IC, resistor, or any other component. Created components are then available for re-use in future designs, decreasing development time. The library is a developing resource at Orbion, and several components present in this project were created and imported into this library to continue building up the available components for future designs.

Altium also features a configuration management system, Altium 365. This was used during this project to backup design files, view their edit history, and be able to access them from different devices – as well as online.

LTspice

LTspice is a free to use SPICE software developed by Analog Devices [14]. SPICE software is extremely helpful for simulating circuits, especially those using ICs or extensive analog circuits. In LTspice, most of the SPICE models of LT-series ICs from Linear Technology are built into the software, making simulations of these ICs very easy to set up and run.

LTspice was used extensively in the 200V DC-DC Converter portion of the project, for simulating the LT8304-1 IC in Chapter 4. It was also used for simulating the analog circuitry present in the Backbone Test Fixture.

Falstad Circuit Simulator

Falstad is a free open-source online circuit simulator [15]. Like LTspice, it is very helpful for analyzing circuits, however it is not a fully-fledged SPICE simulator. Falstad is useful for quick simulations of Resistor-Inductor-Capacitor (RLC) circuits, however not for moe complicated designs such as designs with ICs or needing a specific Zener voltage or a gate-source voltage. Falstad is limited in that sense.

While Falstad is limited in functionality, it was pleasant to use for performing quick simulations of the voltage divider/LPF circuit present in the PPUP002026 Test Fixture.

Rapid Harness

Rapid Harness is a software package used for the creation of ECAD drawings of specifically wiring harnesses [16]. The features included in the software make it simple to place down connectors, create wiring tables, and export the designs for manufacture.

Rapid Harness was used for the DAQ harness design in the PPUP002026 Test Fixture.

LabVIEW

LabVIEW is a widely used systems programming software package developed by National Instruments [17]. LabVIEW provides the ability to design and program control and monitoring interfaces very quickly and easily. LabVIEW features many built-in functions critical for communicating with DAQ systems, as well as all the typical functions expected of a programming language. The interface is entirely graphical, allowing for easy viewing of data flow in the software, as well as quick assembly of user interfaces.

LabVIEW was the software of choice for the PPUP002026 Test Fixture, facilitating the creation of the automated testing software and an easy-to-use interface for managing the automated test.

3.2.2 Design Conventions

3.2.2.1 Schematics

While there is no explicit set of rules for how to draw schematics, Orbion follows industry conventions for creating organized schematics. Following industry conventions is important for creating organized schematics. If a test fixture circuit became very complicated or was going to be used multiple times, a sub-circuit was created to reduce clutter of the higher-level schematic sheet. This type of hierarchical design was utilized for these schematics, as both the PPUP002026 Test Fixture and the Backbone Test Fixture had multiple circuits used more than one time.

All components in the schematics were placed on a 100-mil grid, to keep all connections aligned and wires straight. Circuits were drawn such that the signal path flows from left

to right. Component placement and net routing was done so there is the least possible crossing of nets.

On the main schematic sheet of each design, boxes were placed around groups of components and labeled. Notes were added into schematics for specific application notes, such as how a capacitor needed to be placed next to an IC or for a calculation for an op-amp. These notes aid in the general readability and understanding of the schematics.

Jumpers were implemented in the schematics to facilitate easier design bring-up. Jumpers are not populated during the initial verification process of designs to protect subsequent circuits in case there are any issues. Test points were placed on any net deemed important to the overall function of the design, such as power supply nets or critical signals. Test points allow for easier measurement of signals during the verification process.

3.2.2.2 Electrical Part Selection

First and foremost, components in the design should have an automotive (AEC-Q101, AEC-Q200) or similar high reliability rating, when possible. Components were selected to be an 0603 package or larger to ensure that the boards could be hand-soldered if needed, as anything smaller than an 0603 is difficult to hand-solder. With that said, using too large of a component package could potentially obstruct other components or make the layout difficult. Specific parts within the project such as ICs, diodes, and transformers all are selected on an as-needed basis. The specific requirements for these are per application and will be described in the design descriptions. Part wattage rating depends on package size and tolerance, so the wattage is also selected as-needed per application. Resistors and capacitors were selected based on the criteria specified in Table 1.

Table 1. Specifications for selecting resistors and capacitors.

Specification	**Resistors**	**Capacitors**
Voltage Rating	Highest Possible in the package	
Tolerance	≤ 1% for critical components, ≤ 10% otherwise	
Technology	Thin Film/Thick Film	Ceramic/Solid Tantalum
Preferred Manufacturer	Vishay, Panasonic	KEMET, Kyocera
Notes	Temp. Coeff. < 100PPM/C	Dielectric: X5R, X7R

3.2.2.3 PCB Layout

General Conventions

Layout considerations include choices relating to the size of the PCB, component placement, and the general functionality of the PCB. A majority of the PCB layout conventions are per IPC-2222B, such as signal integrity and manufacturability considerations. Components were placed only on the top side of the PCB to utilize a single solder stencil so the PCB could be assembled in a reflow oven, to make assembly quicker and easier. Components were also strategically placed so that a hand-soldered assembly could be completed if required. For easier readability, component designators

were placed parallel to the bottom edge or right edge of the PCB. Additionally, all silkscreen was placed only on the top side of the PCB for cost reduction of PCB fabrication. Per preference of Orbion, #4-40 holes were used where possible as this hardware is widely available.

Design Rules

In the Altium PCB editor, design rules are also an important factor for creating a proper design. These rules must be input into the PCB editor to meet or exceed the minimum ratings of the manufacturer where the PCBs are built, to guarantee all the electrical clearances in the design. These design rules include tolerances for annular ring, trace width, various clearances, etc.

High Voltage Considerations

The PCBs in this project contain HV signals, up to 200V potential. To prevent the arcing of these HV signals, any HV nets were placed at least 20-mils away from any other net at a different potential. HV is defined as 50V or above for this project.

3.2.2.4 Software

All software development was performed on fully verified test fixture hardware. A bottom-up hierarchical approach was taken for developing the software. The first step in developing the automated software was programming each individual test sequence. Each sequence was programmed as its own LabVIEW Virtual Instrument (VI) file. Similar to the development of the schematics in 3.2.2.1, if a block of code was being used multiple times, they were adapted into their own sub-VI files to adhere to the hierarchical design.

Once all the test sequences and their support codes were developed, a main LabVIEW VI was created containing a state machine which would select which sequence was going to be run. This state machine is the core of the automated software, facilitating all operations of the software.

Lastly, the user interface was developed, implementing the controls for the state machine. For the purposes of this project and to make easy to use software, the controls are limited to a start and stop button, as the entire test is automated. Additionally, the user interface was designed with indicators to indicate the status of the state machine.

3.2.2.5 Design Reviews

Formal design reviews were conducted periodically during the development of all components of the designs to verify that all requirements were being met, no issues were found, and no changes needed to be made.

3.3 Manufacturing

The manufacturing process begins with preparing drawings for the PCBs, PCBA, and harnesses. The drawings contain information about the manufacturing standards and any

special notes for the manufacturer to conform to. While PCB manufacturing was done at a third-party manufacturing plant, conforming to the IPC-6012E [7] standard; PCB assembly and harness manufacturing were both performed in-house at Orbion to IPC-J-STD-001H [8] and IPC/WHMA-620E [9] , respectively. Once all manufacturing was completed, the verification process began.

3.4 Verification

3.4.1 Verification Tools

ESD-Safe Lab Bench

Orbion has constructed several ESD-controlled lab benches for testing purposes of electrical components. The lab benches are all fitted with rubber ESD mats that are grounded to the bench and to the earth ground through a standard electrical outlet. The lab benches were utilized for all testing and verification, to protect the fixtures from ESD events, since the fixtures are ESD sensitive.

Fluke True RMS Multimeter

Several models of Fluke multimeters were used, specifically the Fluke 289 and Fluke 87V models. The multimeters were used for measuring AC and DC voltage, DC current, and resistance. The meters were used for the verification of the 200V Converter and the PPUP002026 Test Fixture. All multimeters were calibrated per ISO/IEC 12025:2017 [18].

Rigol DP832 Power Supply

The DP832 is a DC power supply with two outputs capable of supplying 30V @ 3A, and one output capable of 5V @ 3A. The power supply has adjustable settings for voltage and current limiting. The adjustable settings are designed to turn off the power supply in the event a connected component were to unexpectedly exceed the settings, for safety. The DP832 was utilized during verification of the 200V Converter and the PPUP002026 Test Fixture. The DP832 was calibrated per ISO/IEC 12025:2017 [18].

Keysight DSOX1204G Oscilloscope

The DSOX1204G is a digital storage oscilloscope. The oscilloscope was utilized for viewing startup voltage transients of the PPUP002026 Test Fixture power supplies and for viewing the AC voltage waveforms of the 200V Converter output. The DSOX1204G was calibrated per ISO/IEC 12025:2017 [18].

Clarostat 240-C Power Resistor

The Clarostat 240-C is a power resistor that has an adjustable resistance on a sca1e of 1Ω to 999,999Ω. The Clarostat features six decade steps for changing the resistance. The Clarostat was used during the 200V Converter verification to load the output, and for

setting the minimum load resistances of the power supplies on the PPUP002026 Test Fixture. The 240-C was calibrated per ISO/IEC 12025:2017 [18].

Engineering Model PCBAs

Engineering models of the PCBAs in the PPU are designated for development and testing use and are functionally equivalent to the flight models of PPU PCBAs. These engineering models were utilized to verify the operation of the test fixture, as the engineering model PCBAs imitate the UUTs that the fixture will be testing.

3.4.2 PCBA Verification Methods

The first step in verifying a PCBA is to perform a visual inspection under 10x magnification to verify the PCBA was manufactured properly. Since the reflow oven was utilized for assembly of the PCB, there is a chance that some pins could be bridged or shorted afterwards, so a visual inspection is necessary. The next step is to perform an unpowered Ohm-out. An Ohm-out is an electrical method for verifying there are no undesired electrical shorts that a visual inspection could not detect. A multimeter is used to probe several nets on the PCBA and measure resistances between the nets.

After performing the unpowered visual inspection and Ohm-out, powered electrical testing could begin. The methods for powered verification vary from design to design. However, a general method for the process is first verifying the power supplies are functional, then verifying the next sub-circuit in the chain, and so on and so forth.

3.4.3 Software Verification Methods

Since the LabVIEW software developed in this project is designed to run on physical hardware, the best way to verify the functionality of the software is on the hardware. Initially, the software is verified with only the DAQs connected to the computer, and nothing else. In this phase, using LabVIEW's Highlight Execution feature, the program can be slowly stepped through and each process can be observed carefully. A multimeter and/or oscilloscope is used to verify the analog and digital outputs from the DAQs.

Next, the program is run with the DAQs connected to the test fixture to verify the analog and digital outputs function properly with the PCBA. At this stage, an engineering model PCBA is installed to verify the analog inputs of the DAQs read voltages correctly.

3.5 Conclusion

The project design and verification methods establish the tools, conventions, and procedures used to develop and validate the designs in this project. The next three chapters show the application of the methods to the design and verification of the 200V power supply and test fixtures.

4 A 200V Isolated DC-DC Flyback Converter

4.1 Introduction

The first design will not be a test fixture, but a power supply to be used in the PPUP002026 Test Fixture described in Chapter 5. The PPUP002026 has two power inputs: a 12V and a 200V. The motivation behind designing a 200V Converter is since most commercial off-the-shelf (COTS) power supplies able to deliver HV in a small package cannot deliver enough current to meet the requirements of the PPUP002026 power inputs. This chapter covers the development of the 200V Isolated DC-DC Flyback Converter, a power supply capable of meeting the requirements of the PPUP002026.

4.2 Initial Design Explorations

Early in the design process, the Texas Instruments WEBENCH Power Designer [19] was utilized to find a potential solution for the design of the 200V Converter. The power designer suggested using the Texas Instruments LM2585, a basic flyback controller IC [20]. Using the output from the Power Designer, a simple proto board was soldered together to test the design.

After testing the board, it was clear the LM2585 was not designed for high step-up applications. The switching node was set at a fixed frequency which relied heavily on large output capacitors to sustain the output voltage. Due to this combination, the converter was not able to build the output voltage high enough for use in this project.

While this test was ultimately unsuccessful, it was useful for getting familiar with designing for the flyback topology.

4.3 Designing for the LT8304-1

The failure of the proto-board design in the previous section led to more in-depth research regarding potential controller ICs to use in the design of this converter. The LT8304-1 from Analog Devices [21] was chosen as a good candidate for this design. The LT8304-1 is designed specifically for high step-up applications and contains examples of 200V and 400V supplies in the datasheet. It was also chosen due to the isolated topology, allowing for the HV side of the converter to float if needed. In this section, the details of designing the power supply utilizing the LT8304-1 will be described. This section follows the “Applications Information” section of the LT8304-1 datasheet [21], using the provided equations.

4.3.1 Output Diode

First, the output diode was selected. The diode forward voltage, V_F, is used in following calculations, so it was required to choose this component first. The basic criteria for this diode is as follows:

- Reverse Voltage, V_r, of >250V

- Rectified Current, I_O, of >100mA
- Forward voltage of <1V
- Reverse Recovery Time, t_{RR}, of < 300ns

While this is the minimum acceptable criteria, exceeding these criteria is preferred as doing so will increase the overall performance of the power supply. Selecting a part with a small footprint (however, still hand-solderable) is also preferred as this will help keep the overall size of the power supply as small as possible.

The SBR1U400P1 from Diodes Incorporated [22] was selected. It exceeds all the basic criteria, with following properties:

- $V_r = 400V$
- $I_O = 1.0A$
- $V_F = 0.82V$ (typ)
- $t_{RR} = 85ns$ (max)

4.3.2 Transformer

Next, the transformer is chosen. The LT8304-1 datasheet includes a list of "pre-designed" transformers from different manufactures, which Linear Technology has directly worked with to provide known working solutions. It is preferred to use one of these options, as that will help guarantee the stability of the power supply.

The Applications Information section of the LT8304-1 datasheet suggests minimizing the leakage inductance to prevent voltage spikes. $V_{LEAKAGE}$ is defined as the worst-case voltage spike caused by leakage inductance. With this information, the primary-to-secondary turns ratio, N_{PS}, can be calculated by the following equation:

$$N_{PS} < \frac{150V - V_{IN(MAX)} - V_{LEAKAGE}}{V_{OUT} + V_F} \tag{4.1}$$

Evaluating with $V_{IN(MAX)} = 24V$ and $V_{LEAKAGE} = 40V$, gives a N_{PS} of 0.398, or approximately 1:2.5 turns.

Next, the minimum required primary inductance, L_{PRI}, is calculated. Due to the topology of the LT8304-1, there are minimum inductance requirements for both the switch-on and switch-off times. For the switch-on time, L_{PRI} is calculated by

$$L_{PRI} \geq \frac{t_{ON(MIN)} * V_{IN(MAX)}}{I_{SW(MIN)}} \tag{4.2}$$

where the minimum switch-on time, $t_{ON(MIN)} = 160ns$ and the minimum switch current limit, $I_{SW(MIN)} = 0.48A$. Evaluating this equation gives a minimum inductance of $8\mu H$. Next, using the equation for switch-off time, L_{PRI} is calculated by

$$L_{PRI} \geq \frac{t_{OFF(MIN)} * N_{PS} * (V_{out} + V_F)}{I_{SW(MIN)}} \tag{4.3}$$

where the minimum switch-of time, $t_{OFF(MIN)} = 350ns$. Evaluating gives a minimum inductance of $1.8\mu H$. Since the switch-on inductance is higher, $L_{PRI} = 8\mu H$.

After these calculations, there are three options to choose from the pre-designed transformers list. As all the primary inductances are the same at 40µH, due to the recommendation to have a low leakage inductance, the Wurth Elektronik 750315839 [23] was selected, with the following properties:

- $L_{LKG} = 0.25\ \mu H$
- $L_{PRI} = 40\ \mu H$
- $N_{PS} = 1:10$
- $V_{IN} = 4$ to $36V$
- $V_{OUT} = 200V$

4.3.3 Snubber Circuit

The LT8304-1 datasheet recommends implementing a snubber circuit to clamp $V_{LEAKAGE}$ spikes, dampen switch ringing, and improve EMI performance of the converter. The snubber circuit consists of a RC + DZ pair (Resistor/Capacitor + Schottky/Zener). The Schottky and Zener diode component is determined by the Zener voltage, found by:

$$V_{ZENER(MAX)} \leq 145V - V_{IN(MAX)} \tag{4.4}$$

from the datasheet. Since the maximum input voltage is 24V, the resulting $V_{ZENER(MAX)}$ is 121V. A 110V Zener diode was chosen, specifically the Vishay BZG03C110-M3-08 [24]. For the Schottky, the only criteria is the reverse voltage. Since the internal MOSFET of the LT8304-1 is rated to 150V, the Schottky reverse voltage needs to be at least 150V. The Vishay V1F22HM3/H [25] was chosen, with a reverse voltage of 200V.

For the RC portion of the network, the datasheet recommends starting off with a 100Ω resistor and a 220pF capacitor. These values were not altered for the first revision.

4.3.4 Feedback Resistors

There are two resistors depicted in the block diagram from the LT8304-1, the feedback resistor, R_{FB} and the reference resistor, R_{REF}. The latter shall be set at 10kΩ, as the datasheet states the LT8304-1 is trimmed for this specific value, ±10%. R_{FB} is then calculated by

$$R_{FB} = \frac{R_{REF} * N_{PS} * (V_{OUT} + V_F)}{V_{REF}} \tag{4.5}$$

where $V_{REF} = 1.00V$. Evaluating gives a feedback resistance $V_{FB} = \sim 200k\Omega$.

4.3.5 Output Capacitor

Lastly, the output capacitor was selected. The datasheet recommends sizing the capacitor based upon the desired output ripple, ΔV_{OUT}. The requirement for the output ripple is ≤10V, however reducing the ripple is always better so $\Delta V_{OUT} = 1V$ was chosen. Using the equation

$$C_{OUT} = \frac{L_{PRI} * I_{SW}^2}{2 * V_{OUT} * \Delta V_{OUT}} \tag{4.6}$$

the output capacitance can be calculated. The typical value for $I_{sw} = 2.4A$, so that will be used for this calculation. With a 1V ripple, $C_{OUT} = 0.576\mu F$. Expanding the ripple to 2V gives $C_{OUT} = 0.288\mu F$. Using typical capacitance values, this gives the option of using a 0.33uF or a 0.47uF. The 0.47µF was chosen for the output capacitor.

4.4 Simulation and Prototype

Before investing time into developing a PCB for this design, a SPICE simulation was performed in LTspice. Afterwards, an evaluation PCB of the chip was purchased and modified with the parts selected in the design analysis.

4.4.1 LTspice Simulation

The LTspice simulation was conducted to verify that the calculated components from Section 4.3 would function properly with the LT8304-1. While the exact components are not easily available in LTspice, similar counterparts were selected/designed for simulation purposes. The built in LT8304-1 SPICE model was utilized. Shown in Figure 4.1 is the LTspice simulation schematic. *Cs*, *Rs*, *Ds*, and *Dz* represent the RC + DZ snubber network. The inductors *Lp* and *Ls* represent the transformer. The 1:10 turns ratio translates to a 40µH primary inductance and a 4000µH secondary inductance. The SPICE directive *K1 Lp Ls 1* indicates the two inductors are coupled together, like a transformer. The output capacitor is a single 0.47µF, *Cout*. There is a 100kΩ load resistance, *Rload*, to demand 2mA of current from the converter. The SPICE directive *.tran 100m startup* signifies the simulation is run for 100ms, and all the initial sources are 0V, to simulate turning on a power supply.

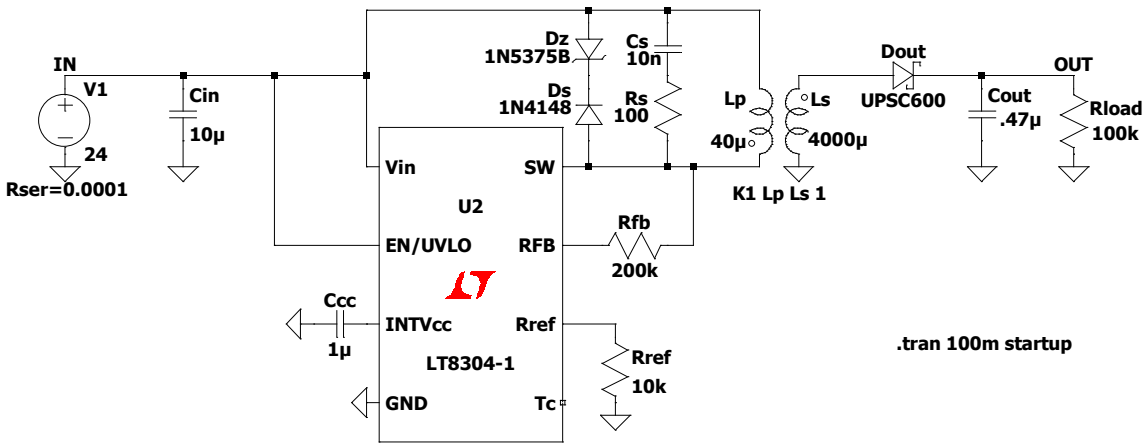

Figure 4.1. LT8304-1 simulation schematic, exported from LTspice.

Figure 4.2 is a section of the V(out) waveform generated from the simulation. The waveform was taken near the end of the 100ms simulation, so the output voltage has settled. The waveform is centered at approximately 202.56V with a low voltage ripple of 120mVpp which is within the requirements for the design.

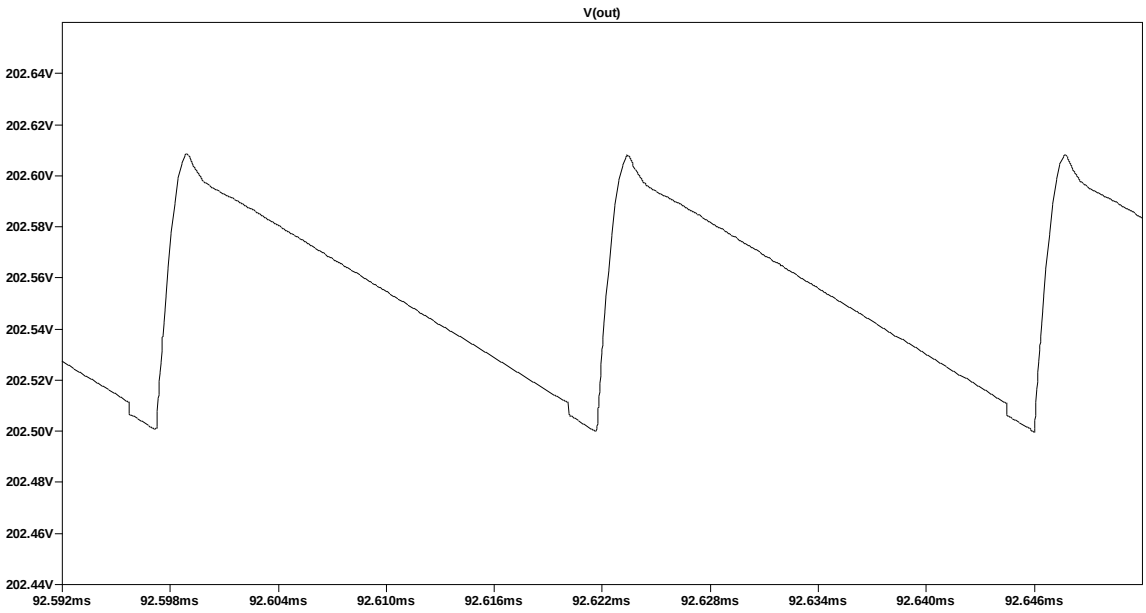

Figure 4.2. Output voltage waveform of the LT8304-1 simulation, exported from LTspice.

4.4.2 Evaluation Board Prototype

Given the success of the simulation, the Linear Technology DC2393A evaluation board was purchased. The evaluation board featured a pre-built circuit with the LT8304, designed for an 8-36V input and 5V output. So, it was set up in a step-down

configuration. To configure the evaluation board for stepping up the input voltage, some modifications needed to be made.

First, all components that were incompatible with the higher voltage design were removed: LT8304, feedback resistor, transformer, output diode, and output capacitors. Afterwards, these components were replaced with the calculated components from Section 4.3. Shown in Figure 4.3 is the modified evaluation board, with voltage probes connected for testing.

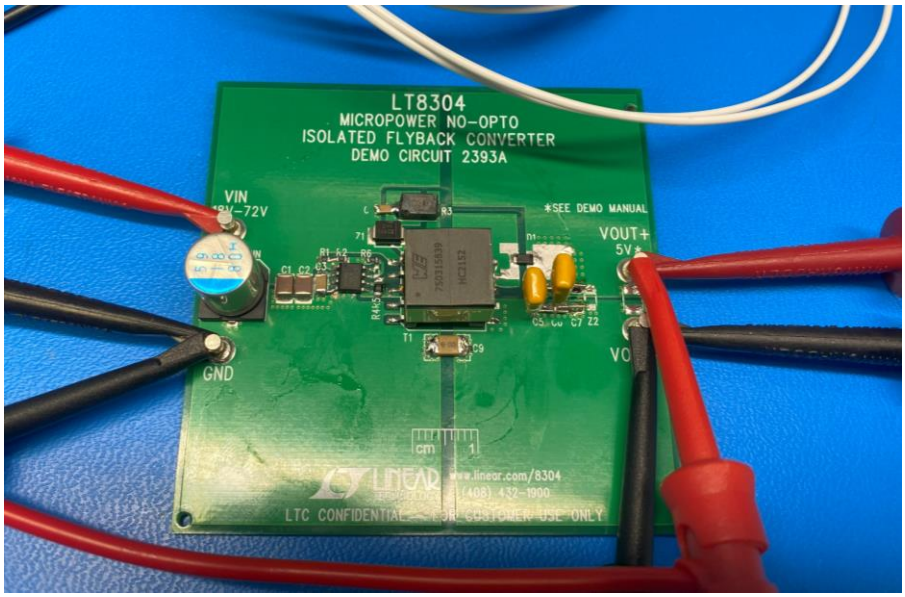

Figure 4.3. Modified DC2393A Demo Board from Linear Technology, with probes attached.

4.5 Revision A1 PCBA

Following the simulation schematic in Figure 4.1, a schematic was drawn in Altium Designer. After drawing the basic structure of the schematic, several extra components were added to make the design complete. A large amount of input capacitance (~70µF) was added to provide enough energy to keep the converter stable in case of a sudden change in output load. A standard 2.56mm pitch 8-pin electrical interface was added for connecting the converter to another PCB. Unlike the simulation schematic, the HV side of the converter was designed to float with its own HV ground. The HV ground was coupled to the low-voltage ground via a 5.6nF capacitor and a TVS diode to suppress any large voltage spikes on the floating side. These components could be omitted from the PCBA if a true floating supply was needed. Overvoltage protection was added to the output in the form of a BJT with a 220V Zener diode connected to the gate of the BJT. A 220kΩ load resistor was also added to the HV side, to provide a minimum load resistance for the supply to prevent the voltage from running away.

A potentiometer was added on the switching node in order allow adjustment and tuning of the output of the converter. Since the resistance is what sets the output voltage, being able to adjust the resistance should allow for the output to be easily adjusted.

Following the general design of the PCB routing present in the evaluation board, the layout was developed. Two #4-40 mounting holes were added for securing the PCB. The 8-pin header was placed on the opposite edge of the PCB. The total size of the PCB was 1.750x1.235 inches. Shown in Figure 4.4 is a fully assembled revision A1 converter.

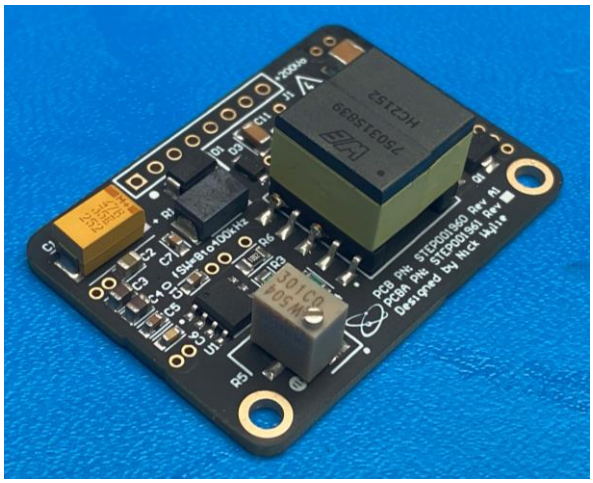

Figure 4.4. Assembled Revision A1 200V Converter.

4.5.1 Results & Discussion

Once manufacturing and assembly of the PCB and PCBA were completed, the design was tested. During testing, the inclusion of the potentiometer was found to have introduced instability in the circuit. While observing the DC voltage of the HV output, if a metallic object such as a screwdriver was moved in proximity of the potentiometer, the output voltage would rise as much as 10 volts above the nominal voltage. When the metallic object was removed, the voltage would decrease. The potentiometer seemed to be acting as an antenna and coupling to the metallic objects, and possibly even to the magnetic field of the transformer.

Using the oscilloscope to observe the output and switching node waveforms revealed the impact of the potentiometer in the converter design. Shown in Figure 4.5 is the AC output ripple (Channel 3, blue) and the DC switching node waveform (Channel 4, red). The LT8304-1 datasheet has example waveforms for what the output and switching node should look like and the switching node is shown to have more oscillations.

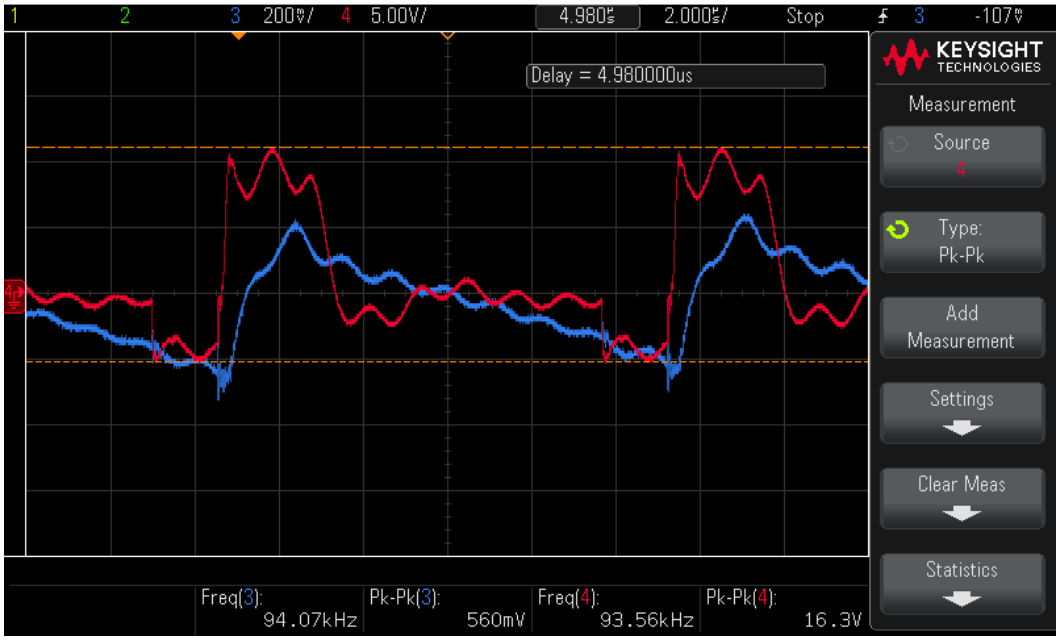

Figure 4.5. Oscilloscope graph of the Revision A1 200V Converter output, (Channel 3, blue) and the switching node (Channel 4, red).

Other issues were found as well: part of the switching node extended trace was routed underneath the transformer, causing degraded performance. The input capacitors were all placed near the LT8304-1 IC and not the transformer, resulting in reduced input power filtering. Lastly, the output capacitor that was chosen was a ceramic capacitor. This capacitor was discovered to be affected by DC bias, effectively halving the output capacitance. Due to these issues, a new revision of the PCB was developed to improve the performance of the converter.

4.6 Revision B1 PCBA

To address the issues found previously, a new revision of the PCBA was designed. Addressing the major issue of the switching node instability, the trace was made as small as possible and was not routed under the transformer. The feedback resistor trace was also made as short as possible with the removal of the potentiometer. The power trace to the transformer was routed more directly, allowing for the input capacitors to be placed in a more beneficial location. The capacitor present in the snubber circuit was also changed from a 220pF to a 10nF part to aid in reducing the oscillations on the switching node. The output capacitor was changed to a 1µF ceramic part. Rather than having only one option, like in Revision A1, an additional footprint was added into the layout to support larger TH film capacitors which are not affected by DC bias. Shown in Figure 4.6 is the new and improved revision B1 PCBA. The full schematic of the revision B1 design can be found in Appendix A.

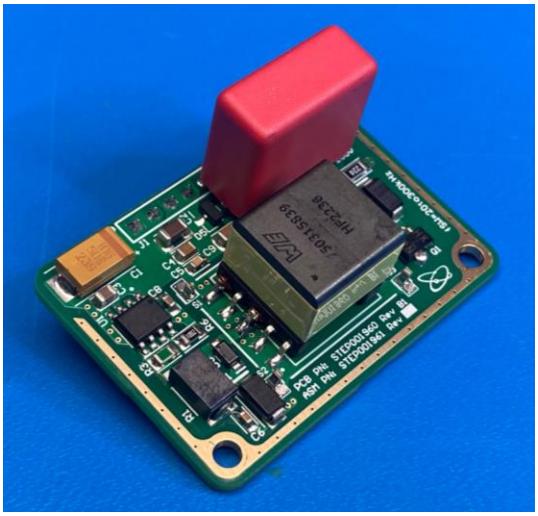

Figure 4.6. Assembled revision B1 200V Converter.

4.6.1 Results & Discussion

After manufacturing the new revision B1 with a 0.33µF film capacitor, the design was tested again. Compared to the revision A1 design, the output voltage AC waveform is almost identical. The switching node oscillations, however, are all gone, and the waveform is representative of what is shown in the datasheet. The converter is shown to be stable, with an output voltage of ~206V and a ripple of <1V.

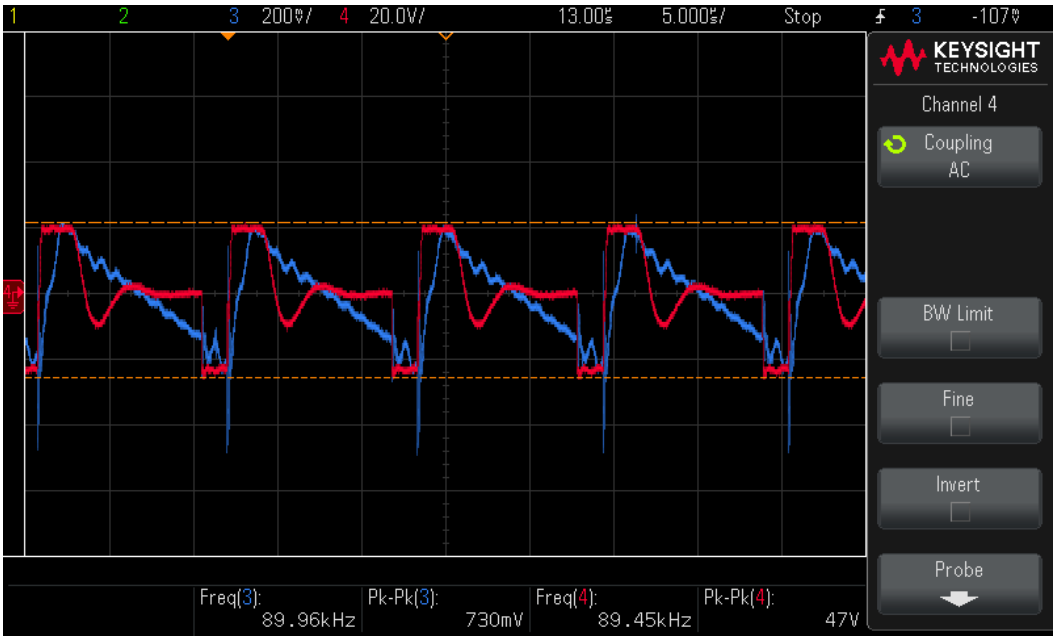

Figure 4.7. Oscilloscope graph of the Revision B1 200V Converter output, (Channel 3, blue) and the switching node (Channel 4, red).

4.7 Conclusion

In conclusion, the revision B1 200V Isolated DC-DC Flyback Converter performed within the performance requirements and did not show any signs of instability. While the design was extensive due to the simulation, prototype, and revision A1 design, it was beneficial to understanding the operation of the LT8304-1. Since the revision B1 design is functional per the requirements, it is ready to be utilized in the PPUP002026 Test Fixture.

5 The PPUP002026 Test Fixture

5.1 Introduction

The PPUP002026 is a PCBA in the PPU featuring three analog cascode amplifiers. Per the PPUP002026 assembly drawing, there are two power inputs, three control signal inputs, and three outputs. This chapter is divided into three distinct sections. First, the design of a PCBA, a DAQ system, a harness, and an automated software program will be detailed, followed by the verification of these design articles. Lastly, the chapter will conclude by presenting and discussing the results of the design and verification processes.

In this chapter, the PPUP002026 PCBA will be referred to as the Unit Under Test (UUT).

5.2 Design

5.2.1 PCBA Design

5.2.1.1 Electrical and Mechanical Interfaces

External Interfaces

There are three external electrical interfaces shown in Figure 5.1. A 5.5x2.1mm barrel jack was chosen as the interface for the standard 24V power adapter (J2), as this is the most common size used at Orbion. For the external DAQ interface (J1), a 15-pin DSUB was chosen. The DSUB is a standard highly reliable connector that is widely used at Orbion, and it will work just fine as a data interface. There is also a CHASSIS connection (SCKT: CHASSIS), which is a soldered banana jack for connecting the fixture to earth ground.

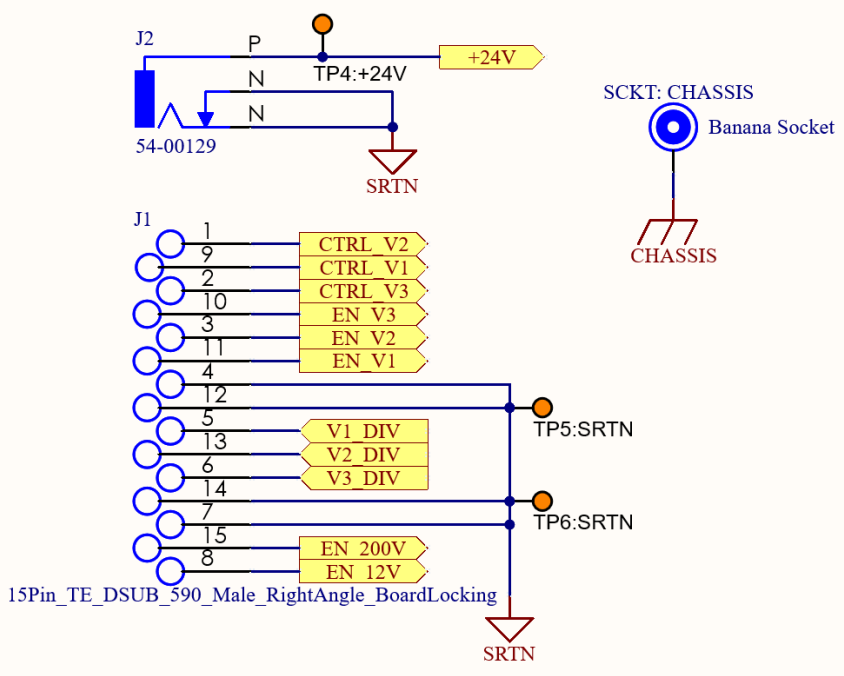

Figure 5.1. Electrical Interface section of the PPUP002026 Test Fixture schematic.

The mechanical interface of the fixture features 16 mounting holes. Six of the mounting holes are #2-56 for the UUT and two are #4-40 for mounting the 200V power supply (as discussed later in this section). The other 8 are #4-40 mounting holes for standoffs or to mount the fixture to a baseplate/enclosure.

UUT Interface

The UUT's electrical interface features gold-plated TH sockets that mate with a pin from another PCBA in the PPU. Using these mating pins on the test fixture would have worked, however it would add a mating cycle to the UUT's sockets. Ideally the sockets would be mated once, to ensure reliability since the UUT is a space-grade PCBA. The pins are also very and would eventually get bent, the gold coating would be lost, and electrical connection would rapidly deteriorate over time due to usage of the fixture. Due to the described reasons, pogo pins were utilized as the electrical interface for the UUT.

The mechanical interface for the UUT is six #2-56 mounting holes. Six standoffs were implemented for the PCBA to mount to, so it could be held down mechanically while contacting the pins. With this, a way to align the PCBA before it contacted the pogo pins was needed. An alignment pin was chosen as the solution. Finding an off the shelf option for this proved to be a challenge however, as the mounting holes for the PPU PCBAs are all #2-56. As it turns out, there is not as wide of a variety of #2-56 hardware as other sizes, such as #4-40. Due to this, custom #2-56 alignment pins were made for three of the six holes, to align the UUT before it contacts the pogo pins. The other three standoffs are for screws to secure the PCBA down for testing.

5.2.1.1 Relay Sub-Circuit

The TE Connectivity IM series relays were selected due to their heritage at Orbion, as they were used in other projects and reported to work well. They are mechanical relays, which isolate their contacts mechanically and are used to completely disconnect the power supplies and electrical loads on the PPUP002026 outputs. They come in many coil voltage ratings, and 2A or 5A contact ratings. The IM03TS, a 5V coil, 2A contact variant, was used for this project.

Shown in Figure 5.2 is the relay sub-circuit section of the schematic. This figure illustrates the relays are powered from a 5V supply. A low-side MOSFET is present to enable or disable the relay, by actuating the "CTRL" signal. There is a 1kΩ resistor and a 50kΩ resistor to prevent ringing and discharge the MOSFET gate, respectively. The circuit also features a diode which dissipates extra energy from the coil caused by inductive avalanche when the circuit is switched off. An LED is also present to indicate when the relay is switched on.

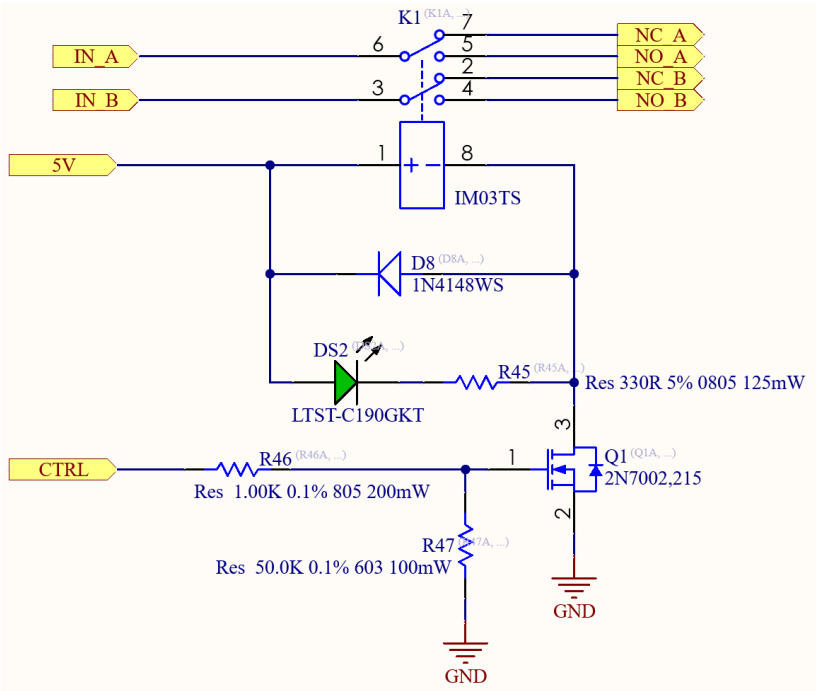

Figure 5.2. Relay sub-circuit section of the PPUP002026 Test Fixture schematic, including a status LED and MOSFET control switch.

5.2.1.2 Power Supply Design

12V Power Supply

A 12V power supply is required per the PPUP002026 Assembly drawing for powering the UUT. The CUI PCN2-S24-S12-S [26] was selected for the 12V supply because it outputs 12V @ 167mA, which exceeds the requirements of the assembly drawing.

For the DAQ system to be able to turn the supply on and off, the PCN2-S24-S12-S was connected to the normally open (NO) contact of a Relay Sub-circuit. This way, when the relay is not receiving a HIGH signal, the 12V supply is off. A 1Ω resistor was placed at the input to the relay to control inrush current. Input and output capacitance was also added before the resistor and on the output of the power supply. A load resistor is present on the output in case a minimum load is needed to keep the supply regulated. Shown in Figure 5.3 is the 12V supply section of the PPUP002026 Test Fixture schematic.

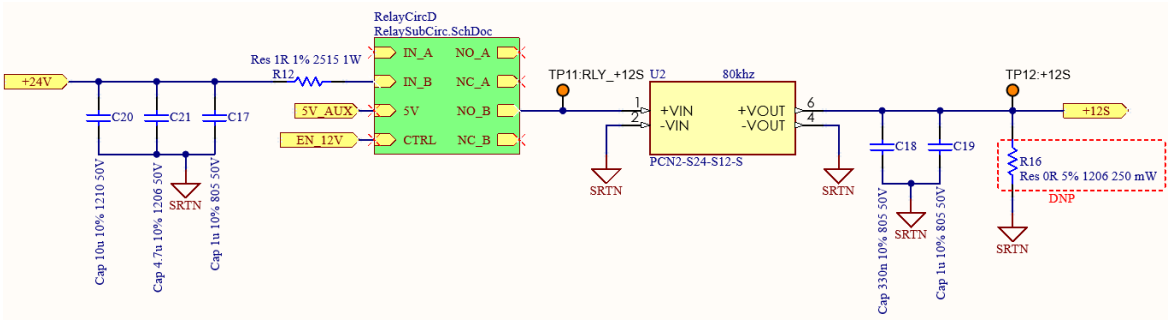

Figure 5.3. 12V Power Supply section of the PPUP002026 Test Fixture schematic, including input filtering, a relay sub-circuit, and output filtering.

200V Power Supply

A 200V power supply is also required per the PPUP002026 Assembly drawing for powering the UUT. This power supply was developed in Chapter 4, requiring an output of 200V ±10V @ 10mA. Like the 12V supply design, the 200V supply is also connected to the NO contact of a relay. A 9Ω current limiting resistor is placed before the relay due to the high amount of capacitance present on the 200V daughterboard. Additional input capacitance was added before the resistor. There is no output capacitance present as it could interfere with the performance of the 200V supply. Shown in Figure 5.4 is the 200V supply section of the PPUP002026 Test Fixture schematic.

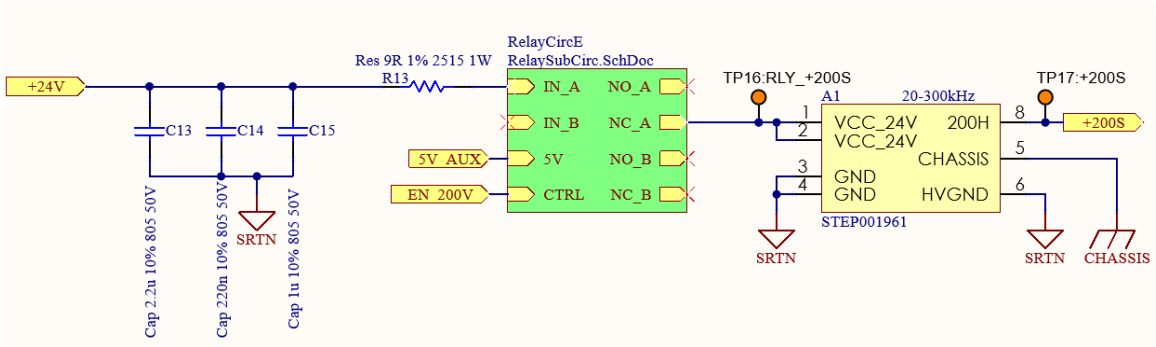

Figure 5.4. 200V Power Supply section of the PPUP002026 Test Fixture schematic, including input filtering, a relay sub-circuit, and the 200V DC-DC Converter.

5V Power Supply

Lastly, a 5V “auxiliary” power supply is required for powering the relays and LEDs in this PCBA. Each relay circuit will draw around ~40mA of current from a 5V supply, when activated. Since there are five relay circuits present in this design, a 5V supply capable of delivering at least 200mA of current is required. The CUI PQP3-D24-S5-M [27] was chosen for this design, delivering 5V @ 600mA. A relay on/off control is not required for this power supply, as it is not connected to the UUT, and is the supply that powers the relays.

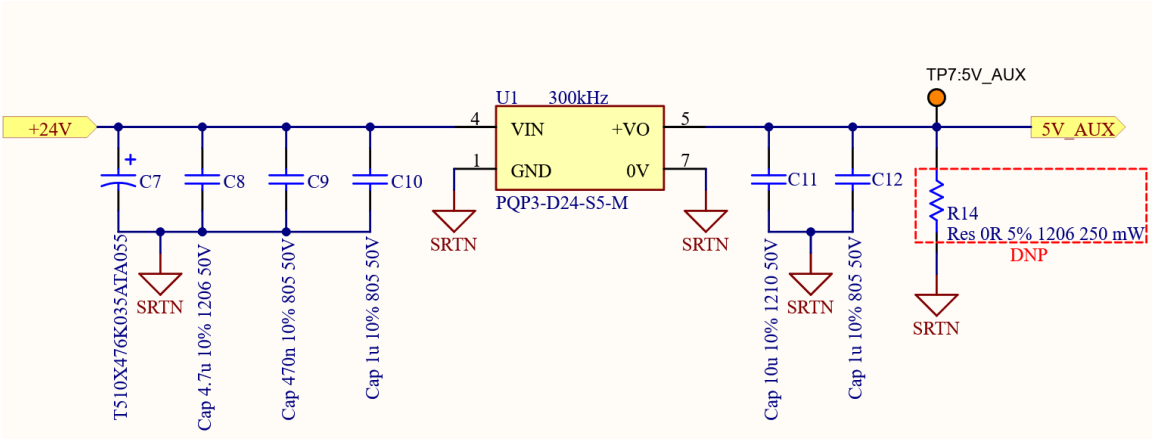

Figure 5.5. 5V Power Supply section of the PPUP002026 Test Fixture schematic, including input and output filtering.

5.2.1.3 Voltage Divider and LPF Design

The voltage outputs from the PPUP002026 exceed the maximum rating of the USB-6002 DAQ (Discussed later in this chapter). The DAQ analog input voltage range is -10 to 10V. To reduce the voltage to the DAQ input range, a voltage divider is used. A low-pass-filter (LPF) is also used to filter out any high frequency noise from the DAQ inputs. Shown in Figure 5.6 is the voltage divider and LPF from the PPUP002026 Test Fixture schematics. Three identical circuits are present in the schematic: one for each output of the PPUP002026.

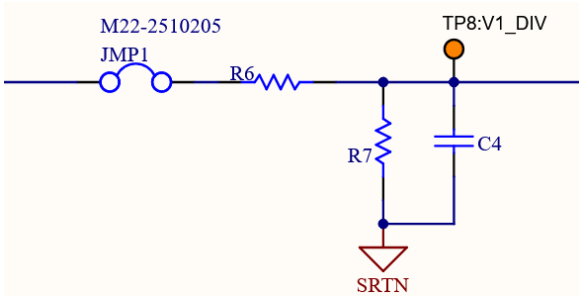

Figure 5.6. Resistor Divider and LPF section of the PPUP002026 Test Fixture schematic. (Component values omitted).

The output voltage of a voltage divider is calculated by

$$V_{out} = \frac{R2}{R1 + R2} * V_{in} \tag{5.1}$$

where R1 and R2 are represented by R6 and R7 in Figure 5.6. The cutoff frequency of the LPF is calculated by

$$f_{cutoff} = \frac{1}{2\pi RC} \tag{5.2}$$

where R is represented by R6 in Figure 5.6. The cutoff frequency should be at least five times higher than the expected measurement frequency to prevent any sampling issues in the DAQ system.

5.2.1.4 The "Zap-Trap"

The "Zap-Trap" used in this design is a standard configuration used on several Orbion PCBAs. Four components make up the "Zap-Trap": two opposing diodes, a capacitor, and a resistor. The two diodes prevent the voltage potential between GND and CHASSIS from exceeding a diode drop. The capacitor acts as a ground filter to bypass AC ground noise from GND to CHASSIS. The resistor aids in the function of this ground filter and was not populated in this design for reasons related to the operation of the PPUP002026.

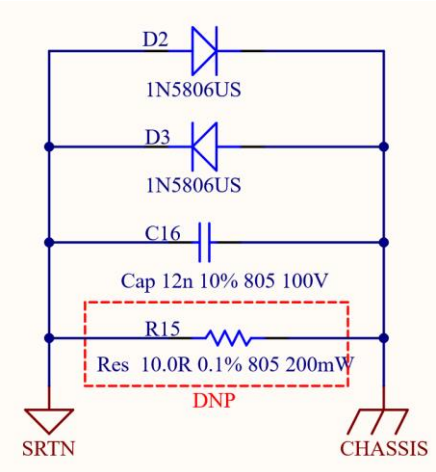

Figure 5.7. "Zap-Trap" section of the PPUP002026 Test Fixture Schematic, including two opposing diodes and an RC filter.

5.2.2 DAQ and Harness Design

5.2.2.1 Choosing the DAQ

The USB series of National Instruments DAQs were chosen for this project, specifically the USB-6002 [28]. This DAQ has an adequate number of analog and digital I/O for the project. The 6002 was chosen over the lower cost USB-6001 because it had two extra bits of analog resolution, for more accurate readings (12 bits vs 14 bits). Two of the USB-6002 DAQs are needed, as there are 3 control signals, and each DAQ only has two analog outputs. The DAQs feature two screw terminal blocks, for connecting all the digital and analog I/O to other devices, and a USB port for connecting to a computer.

One of the tradeoffs with choosing the USB series of DAQs over a more feature-rich chassis-style DAQ is the USB DAQs do not support hardware timing across multiple DAQs. This makes the LabVIEW programming more difficult later in this chapter, however the cost savings on the equipment makes up for the difficulty.

5.2.2.2 Designing the Harness

The harness in this project needed to connect three things together: both DAQs and the PCBA. For the PCBA interface, a mating DSUB was used. For the two DAQs, ferrules were used to provide a good electrical connection to the screw terminals. Using ferrules instead of bare wire will ensure longevity, so these can be taken apart and serviced, without needing to re-strip wire. The full drawing of the harness with connection tables, bundling layout, and wire labels can be found in Appendix B.

5.2.3 Software Design

The automated testing software was developed to automatically perform the amplifier circuit verification tests for a PPUP002026 UUT. The software performs various tests on the UUT, records data from the UUT, and compares the recorded data to the acceptable limits specified in the PPUP002026 assembly drawing.

During these tests, data is recorded and saved in an Excel document, along with an indicator for if the UUT passed or failed the test cases. If a case fails, the software will exit early, to prevent catastrophic damage to the UUT or Test Fixture.

The software was designed to perform an additional, non-critical data collection step, where a sine wave was applied to each control input. This data was recorded; however, it was not checked against any requirements. The data is purely for future UUT failure analysis if required.

As part of the hierarchical design, many VIs were created to organize all of the support code and test sequences. While not every VI is shown in this design section, the most fundamental VIs are discussed. There are three categories of VIs in the software design: building blocks/support code, test sequences, and the state machine.

5.2.3.1 Building Blocks & Support Code

This section outlines the lowest-level VIs in the software. Building blocks/support code includes VIs that read and write voltages on the DAQ channels. Other key features within this category include turning relays on/off and computing the min/max of a sub array. These VIs are essential to the functionality of the automated software.

3-Channel Analog Voltage Write (3ch_vWrite.vi)

This VI writes to three analog voltage output channels. It has a 1D array input and no outputs. The input array, which is split and type casted into two DAQmx Write blocks, contains the voltage values to write to the analog channels. Because two DAQs are used in this design and hardware timing between DAQs is not available, the voltages are written to the outputs at slightly different times. This portion of the software was not required to do any specific timing, so the absence of hardware timing was acceptable. The block diagram for this VI is shown in Figure 5.8. This VI is used several times in the software, whenever a control voltage needs to be applied to the analog outputs (except for the transient test sequence), and whenever the voltage needs to be set back to 0V.

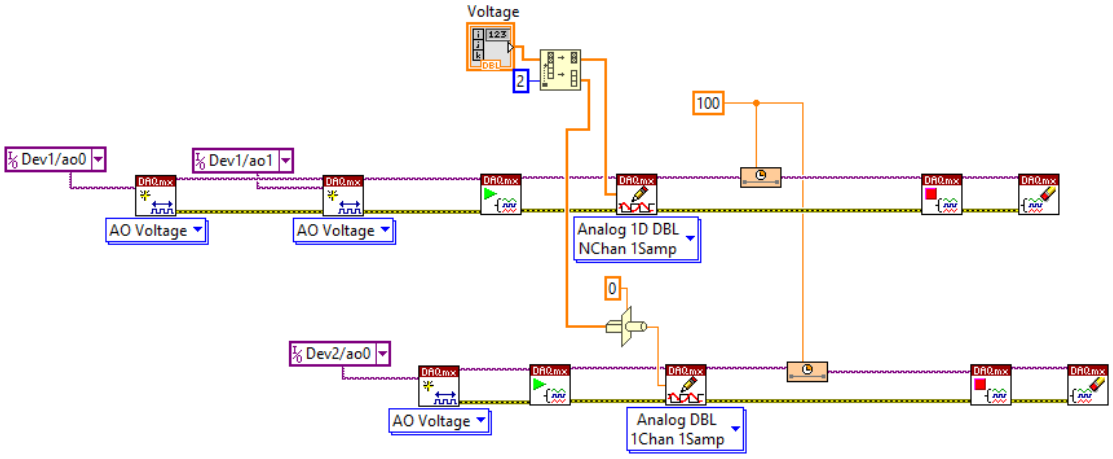

Figure 5.8. 3ch_vWrite.vi Block Diagram. From left to right: analog output channels are selected, the DAQmx task is started, the voltage is output, and the DAQmx task is closed.

6-Channel Analog Voltage Read (6ch_vRead.vi)

This VI reads a finite number of samples from six analog voltage input channels. It has two inputs: the total number of samples per channel and the sample rate (samples/second). The VI outputs a 2D array containing the voltages read from all six channels. This array contains readings from the analog outputs, as well as the PPUP002026 outputs. The PPUP002026 readings (Dev1/ai0-ai2) are split from the main array, then multiplied by the gain of the resistor divider from 5.2.1.3 to output a properly scaled value. The block diagram for this VI is shown in. This VI is used during every data collection step, recording all data to an array (except for the transient test sequence).

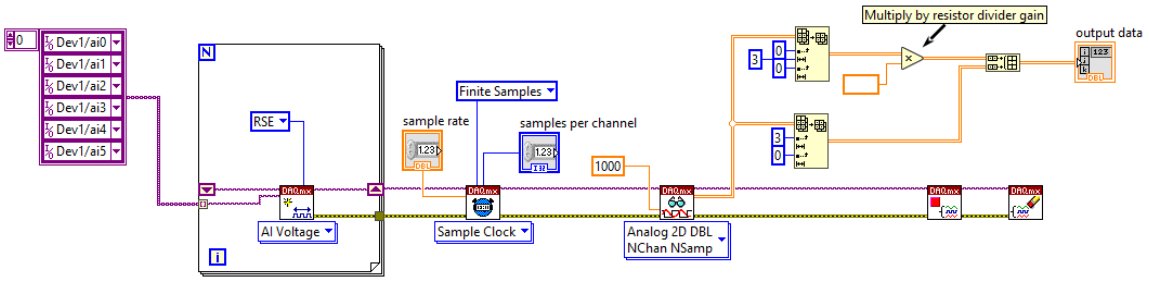

Figure 5.9. 6ch_vRead.vi Block Diagram. From left to right: the analog input channels are selected, the sample clock is set, the voltages are read, the DAQmx task is closed, and the input data is output.

1-Channel Sine Write, 6-Channel Read (1ch_SineWrite-6ch_vRead.vi)

This VI performs two functions; a sine wave voltage output and a six-channel voltage read. For the six-channel voltage read functionality, this VI utilizes the exact same logic as described in the previous 6ch_vRead.vi section. This VI has six inputs: the analog output channel, sample rate, number of samples per channel, amplitude, frequency, and offset. The sine wave is generated using a sample clock to time the sample generation and a LabVIEW sine generator VI, utilizing all six inputs. The voltage read utilizes the same sample rate and samples per channel to keep the data acquisition synced with the sine wave output. The DAQmx Write and Read blocks are both placed in a LabVIEW flat sequence, to time the start of the generation of the waveform exactly with the start of the reading of the voltages. The block diagram for this VI is shown in Figure 5.10. This VI is used specifically for the transient test sequence.

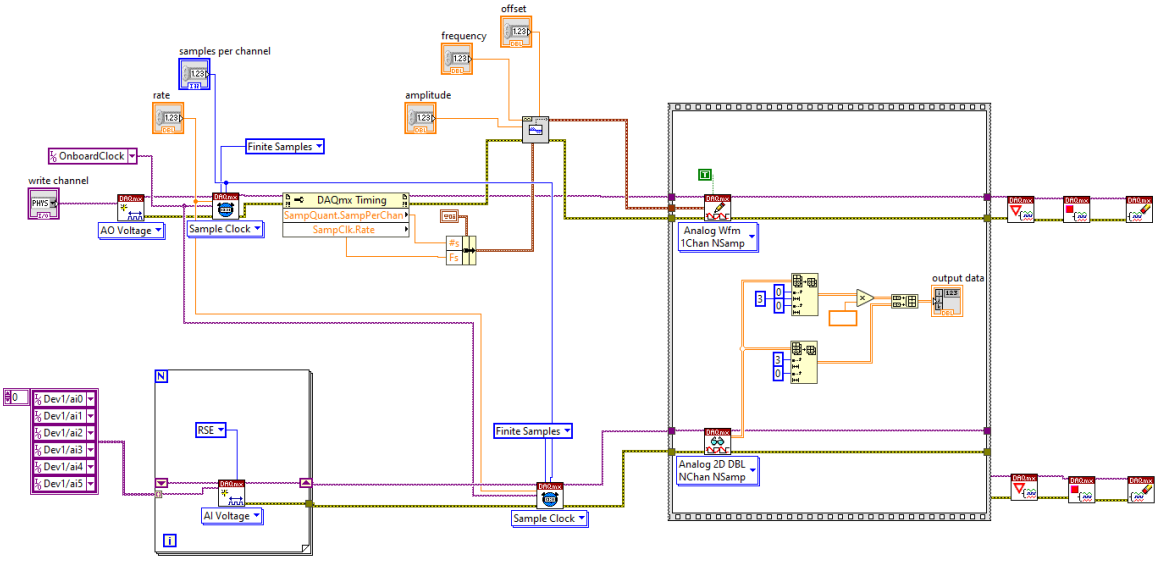

Figure 5.10. 1ch_SineWrite-6ch_vRead.vi Block Diagram. The top portion of the diagram features the sine wave generation, utilizing a sample clock and sine generation VI. The bottom portion features a similar circuit to the 6ch_vRead.vi.

Min-Max of Subarray (MinMaxOfSubArray.vi)

This VI finds the min and max of a given array. This VI inputs a 1D or 2D array, an input indicating which row to select, and a min and max boundary. It has a single Boolean output. Once the VI finds the min and max values of the selected row, it compares them to the input min and max limits. If the values are within limits, the output will be true, otherwise the output is false. The block diagram for this VI is shown in Figure 5.11. This VI is utilized several times in the software, for all the pall/fail criteria checks.

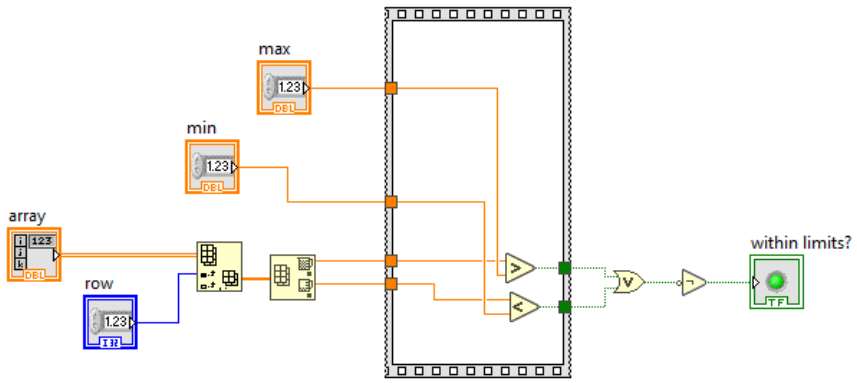

Figure 5.11. MinMaxOfSubArray.vi Block Diagram. The array, row, min, and max values are input, compared in a LabVIEW flat sequence to time the logic, and output to an indicator.

Setting Relays (SetRelays.vi)

Lastly, this VI sets the relay configuration via the digital output port0. It has a 1D array input of Boolean values, indicating which relays are on and off. There are no outputs. Using a DAQmx Write block, the input values are written to the digital port. The block diagram is shown in Figure 5.12. This VI is used several times in the software, to set the relay configuration during all test sequences.

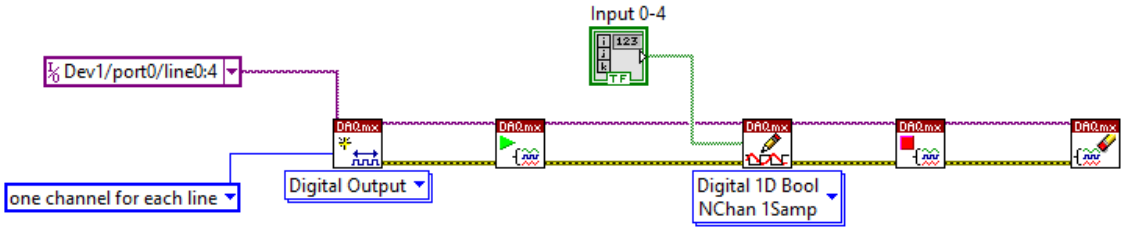

Figure 5.12. SetRelays.vi Block Diagram. From left to right; the digital output port is selected, the data is output, and the DAQmx task is closed.

5.2.3.2 Test Sequences

This section describes the three types of test sequences used in the software. The test sequences category includes the main files that outline the functional tests. These VIs are responsible for setting the inputs, recording the outputs, and passing the recorded data into an Excel report file. The generic format for a test sequence is shown in Figure 5.13. From left to right, the report template is first passed into the VI. Next, the conditions of the test are set with SetRelays.vi and 3ch_vWrite.vi. After waiting for steady state to be achieved, the 6ch_vRead.vi file is used to read in data from the six analog inputs. This data is simultaneously saved into the excel report and compared with the testing limits by MinMaxOfSubArray.vi. Afterwards, the sequence may perform another test case, or the sequence may end and pass the report out.

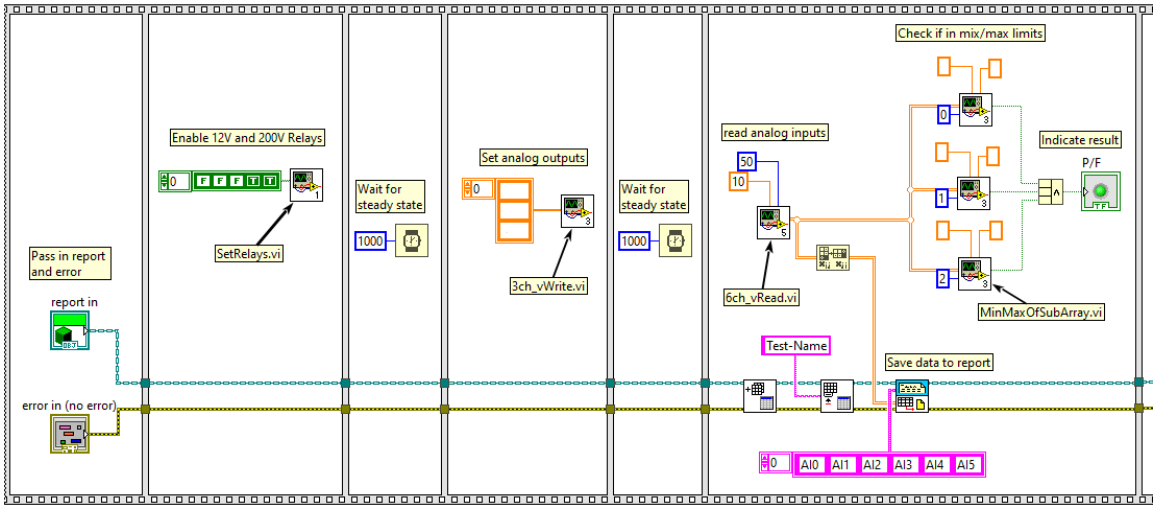

Figure 5.13. Generic block diagram for a test sequence, using a LabVIEW flat sequence.

Power Verification

The purpose of the power verification sequence is to power the UUT with no control voltage inputs. This test sequence starts by turning on the 12V supply, then measuring the three analog outputs. Next, the 200V supply is enabled and the analog outputs are measured again. Last, both supplies are disabled and the sequence ends.

IO Verification

The IO verification sequence is the main functional test for the UUT. A total of 18 test cases are completed in this sequence. First, both power supplies are enabled. Next, the software applies control voltages to the UUT at three different set points on all three inputs and records the analog outputs at each set point. The power supplies are then turned off, the electrical loads are enabled, then the power supplies are turned back on. The next half of the test cases use the same structure as before with the only difference being that the electrical loads are enabled, and all analog output data is recorded. Lastly,

the power supplies are turned off first, followed by the electrical loads, then the test sequence ends.

Transient Data Recording

The transient sequence performs non-critical data collection of a sine wave being applied to the UUT control inputs. In this sequence, both power supplies are enabled first. Next, a sine wave is input into each control input and data is recorded. The power supplies are then turned off, the electrical loads are enabled, then the power supplies are turned back on. The same sine wave input is applied to all the control inputs again and data is recorded. Lastly, the power supplies are turned off first, followed by the electrical loads, then the test sequence ends.

5.2.3.3 State Machine Implementation

The state machine category only applies to the main program VI. This is the topmost level of the program, facilitating the main state machine that selects which tests are run. Shown in Figure 5.14 is the flowchart for the state machine design in the automated software. In the LabVIEW code, the state machine is created with a case structure encapsulated inside of a while loop, per the LabVIEW state machine documentation [29].

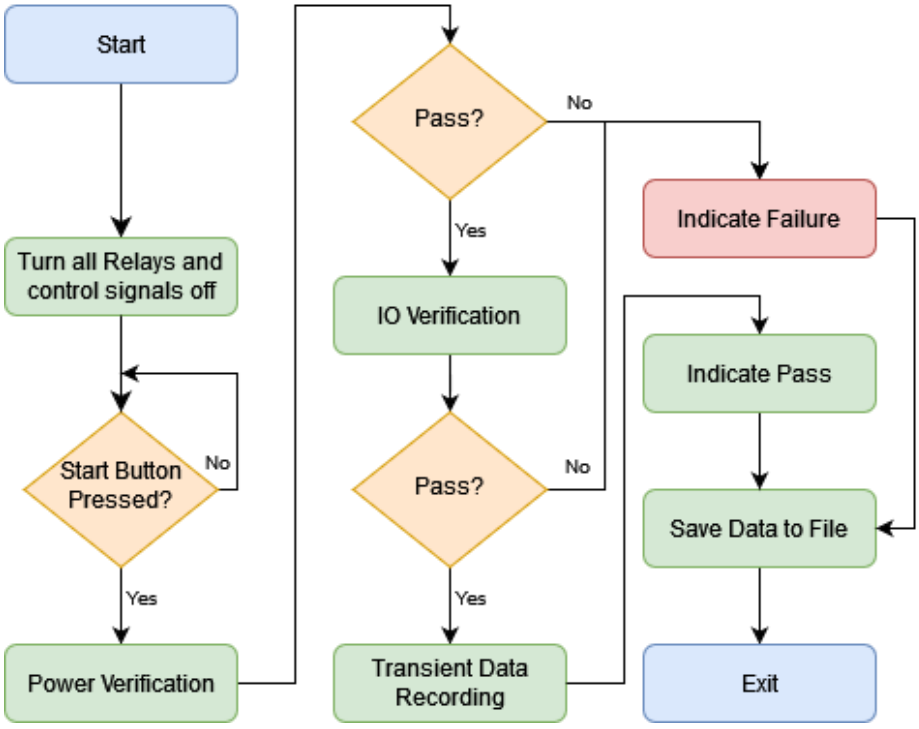

Figure 5.14. State Machine flowchart.

When the LabVIEW program starts, the state machine enters the “Default” case, which ensures all relay circuits are turned off and all control signals are set to 0V. Next, the program moves to the “Wait” case where the program indicates to the operator that the

UUT is safe to be installed. The program will stay in this case indefinitely until the "Begin Test" button is pressed by the operator.

Once the operator starts the test, the program indicates on the user interface that the test is active and enters the "Power Verification" case where the Power Verification Test Sequence is run. This case includes code that will exit the program if any test cases fail in the sequence. Next, the program proceeds to the "IO Verification" case and runs the IO Verification Test Sequence. This case includes code that will exit the program if any test cases fail in the sequence. To run the last test sequence, the program enters the "Transient Data Recording" case where the Transient Data Recording Test Sequence is run. This case does not include any checks to exit the program early, as there are no test cases in the sequence.

The last case in the state machine is the "Save Report" case. This case compiles the data recorded from the three test sequences and saves the data to a single Excel file, with different sheets for each test. A cover sheet is added to the file indicating if all the cases passed. In addition to saving the report, this case also indicates to the operator in the user interface whether the UUT passed or failed the test, and that the UUT can be removed from the fixture.

5.2.3.4 User Interface

The user interface, shown in Figure 5.15, was designed to be operator-friendly, easy to use, and easy to understand. At the top of the interface, the software name and version are listed for easy reference. The left side has large, clearly marked "Begin Test" and "Stop" buttons for the operator to control the test. The right side has five indicator lights, that will illuminate based on the state of the state machine.

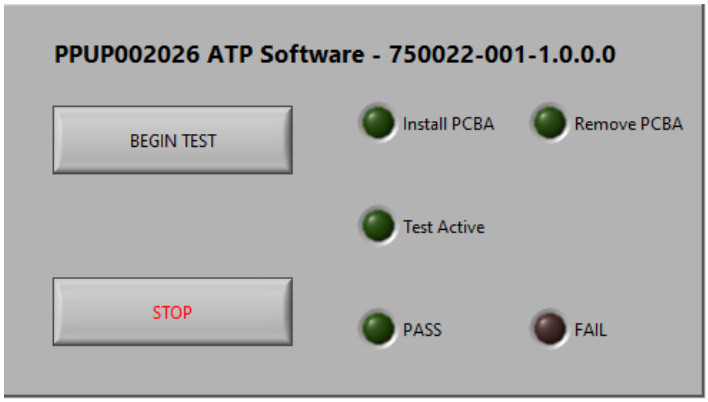

Figure 5.15. User interface for the PPUP002026 automated test software, captured from LabVIEW.

5.3 Verification

5.3.1 PCBA

A formal test procedure outlining the specific steps for verification of the PCBA was written and performed. After performing a visual inspection and Ohm-out, the PCBA CHASSIS banana jack was connected to earth ground. The next step in the procedure was to connect the 24V supply to the barrel jack, but not the AC outlet, so the PCBA is still unpowered. Next, the oscilloscope was connected to the 24V, 5V, 12V, and 200V test points and set to trigger on a rising edge to capture the start-up waveforms of the power supplies. The observation of these rising waveforms was to verify there is no overshoot of the voltages. Afterwards, the multimeter was utilized to verify the static voltages of the power supplies. Once the power supplies were verified, a 3V input was applied to each of the relay control pins to verify the actuation of each circuit.

5.3.2 Software

Software verification was performed on the verified fixture PCBA using a multimeter and standalone power supply to emulate the presence of a UUT to the following requirements:

- Analog voltage outputs do not exceed the input voltage specification per the PPUP002026 PCB Assembly drawing.
- All digital relay control outputs are properly sequenced.
- All DAQ analog inputs read accurate and correct voltage ranges of 0V to 10V when a voltage is applied through the voltage dividers.
- The UUT output voltage PASS/FAIL criteria was correctly implemented per the PPUP002026 PCB Assembly drawing.
- The state machine will exit if any test case fails.
- All recorded data was saved into the MS Excel report for export.

By verifying the PPUP002026 Test Fixture automated software met these requirements, it is proven the software is mature for use to perform functional testing on PPUP002026 hardware. Therefore, a known working engineering model PPUP002026 PCBA was installed onto the test fixture and the automated software test was performed. The fixture passed the engineering model, and the recorded data matched testing data from previous manual testing, further proving the functionality of the fixture.

After the success of the engineering model PCBA, two other PPUP002026 PCBAs were tested, however these were development boards that had just finished assembly and had not gone through any prior testing. The recorded data from both boards fell within the acceptance ranges for all tests, and the software passed both PCBAs.

5.4 Results & Discussion

Based upon the verification performed in the previous section, the PPUP002026 Test Fixture overall performed as designed.

The mounting mechanism with the alignment pins and pogo pins kept the PCBA aligned before contacting the pogo pins and did not damage the UUT. All pogo pins made exceptional contact with the UUT, providing an adequate electrical connection. Shown in Figure 5.16 is the mechanical and electrical interface for the UUT on the PPUP002026 Test Fixture.

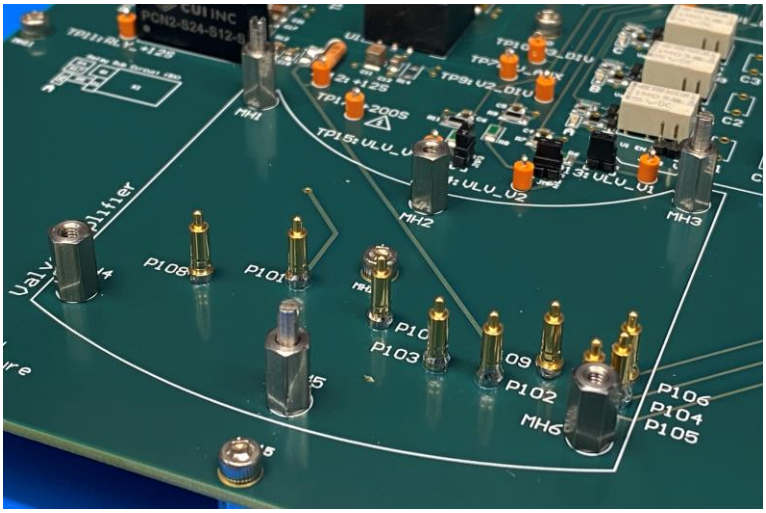

Figure 5.16. UUT Electrical and Mechanical mounting mechanism on the PPUP002026 Test Fixture.

The 5V power supply worked as designed with no voltage overshoot or stability issues. The 12V supply needed a 200kΩ load resistor installed to regulate within specification. The 200V supply functioned as designed, with no issues per the results of Section 4.6.1, however the relay connected to the 200V circuit did not. The relay became welded due to the heat generated by the inrush current of the converter, preventing the converter from being turned off. The relay was removed and replaced with a 5A rated version of the IM series relay. Afterwards, the relay was able to switch the 200V converter on and off with no issues. All other relay circuits performed as designed.

The automated software was tested in three ways: without a UUT, with a known-working UUT, and with two blind tests. When testing with the standalone power supply, voltages exceeding the high and low acceptance ranges for the test sequences were input at the pogo pins. Each individual test sequence was executed separately and caught all values exceeding the ranges, failed the test, and exited the program early. The software successfully met its requirements without the UUT installed, proving that no electrical damage would be inhibited to PPUP002026 hardware.

The automated software was then test-run using an engineering model PPUP002026 and functioned as designed, passing the known-working engineering model. The two blind tests were performed on PPUP002026 hardware that had not been previously tested. Both PCBAs were passed by the software. All data from these three tests were thoroughly analyzed, and the responsible engineer for the PPUP002026 determined all boards did in fact pass testing.

While testing a known-bad PPUP002026 would have been desirable and informative to the performance of the test fixture, no known-bad boards existed at the time, and it was not permitted to intentionally damage any hardware.

Shown in Figure 5.17 is the complete assembled PPUP002026 Test Fixture setup, with the PCBA, harness, DAQs, and USB cables to connect to a computer.

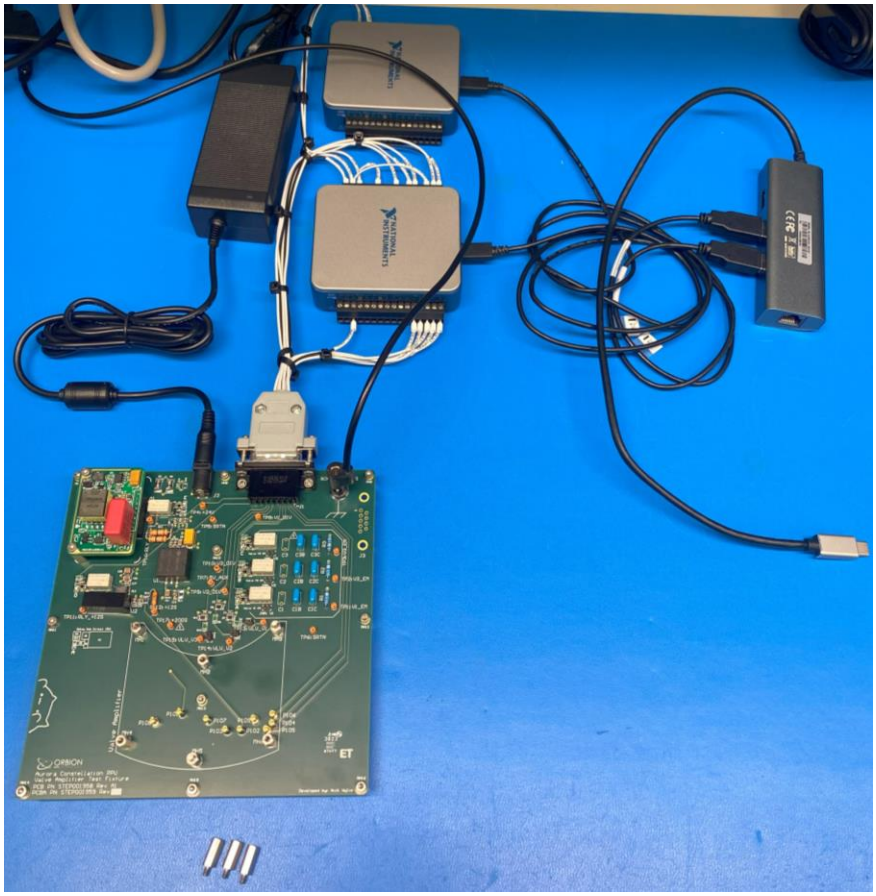

Figure 5.17. Complete test setup of the PPUP002026 Test Fixture. PCBA, Harness, DAQs, and DC supply shown. USB cables present to connect to computer.

5.5 Conclusion & Future Work

In conclusion, the PPUP002026 Test Fixture was successfully designed to the requirements. The PBCA and harness for the test fixture both performed on the first revision, with the only functional issues contained to one relay. This issue was resolved by replacing the relay with a higher current version. The automated software controlled the fixture successfully and provided an easy to use interface for an operator to control the test.

While the fixture did perform as expected for the standalone testing as well as with the three UUTs, more testing should be considered to fully characterize the design. As the PPUP002026 PCBAs are a high-value Space Rated part, a Failure Mode & Effects Analysis (FMEA) should be performed to identify potential risks in the design where the UUT or Fixture could be damaged electrically, mechanically, or cosmetically during the test process. While this fixture performed admirably for simple bench testing, it is not yet proven to be ready to use in a manufacturing environment. Some potential risks of the current design have been identified and include:

- Mounting mechanism allows for user error and risks potential damage to the UUT by scraping parts against the standoffs or pogo pins.
- No automated way to verify all pogo pins are electrically connected to the UUT. A visual inspection and/or probing with a multimeter is required to verify no open circuits.
- Over and under voltage is possible on the components as there is no shutdown feature on the fixture for the 12V and 200V power rails if they fall out of range.
- No long term or environmental testing was performed on the test fixture, so the effects of component aging and wear has not been thoroughly tested.

Acting on these identified risks is critical for long term reliability and performance of the fixture, and to ensure all PCBAs tested with it are not damaged. Orbion has determined for the purposes of this design, the fixture is mature enough to be used with PPUP002026 hardware, however only in a lab environment until the FMEA and manufacturing qualification is completed.

6 The Backbone Test Fixture

6.1 Introduction

The PPUP002046, PPUP002048, and PPUP002085 are PCBAs present in the "Backbone" of the PPU. Each PCBA features different analog circuits, containing MOSFETs, diodes, and ICs, as well as resistors and capacitors. This chapter details the design of a test fixture capable of testing all three PCBAs. First, a display of the new text fixture design using new and old circuits is detailed. Lastly, the chapter concludes by discussing future intentions of the design and verification of the test fixture.

6.2 PCBA Design

This section discusses the design of the PCBA for the Backbone Test Fixture. The design of this PCBA features a few similarities with the PPUP002026 Test Fixture. The external power and data interfaces, 5V power supply, and relay sub-circuit are all identical between the two fixtures. New design features such as the boost converter, buck converter, and MOSFET timing circuits will be detailed. Shown in Figure 6.1 is the electrical block diagram for the Backbone Test Fixture.

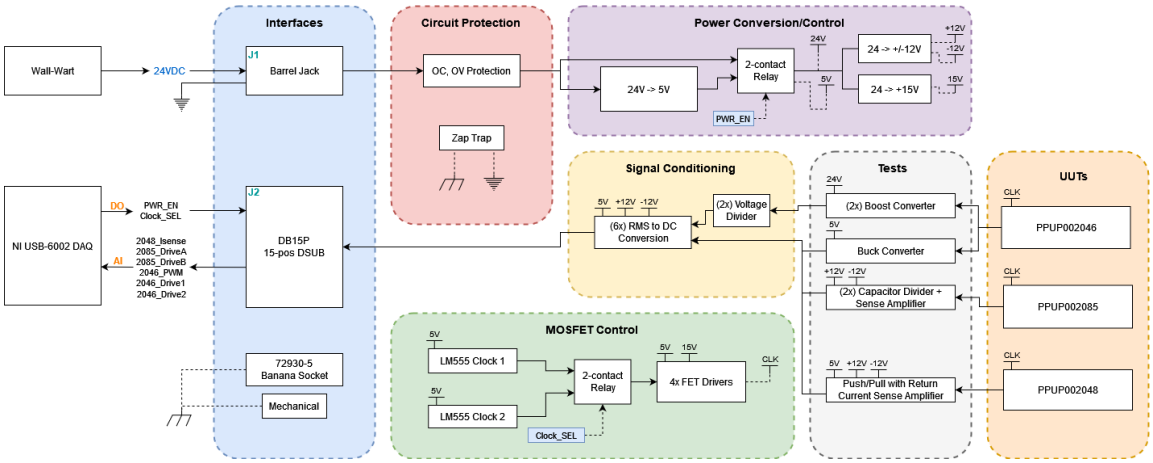

Figure 6.1. Backbone Test Fixture electrical block diagram.

6.2.1 Electrical and Mechanical Interfaces

External Interfaces

There are three external electrical interfaces shown in Figure 6.2. Like those described in Section 5.2.1.1, a 5.5x2.1mm barrel jack, a 15-pin DSUB, and a banana jack are used for the interfaces. The one difference between the two is the DSUB pinout. The mechanical interface for the fixture features 32 mounting holes: 17 of which are #2-56 for the three UUTs, and 15 are #4-40 for standoffs for the fixture.

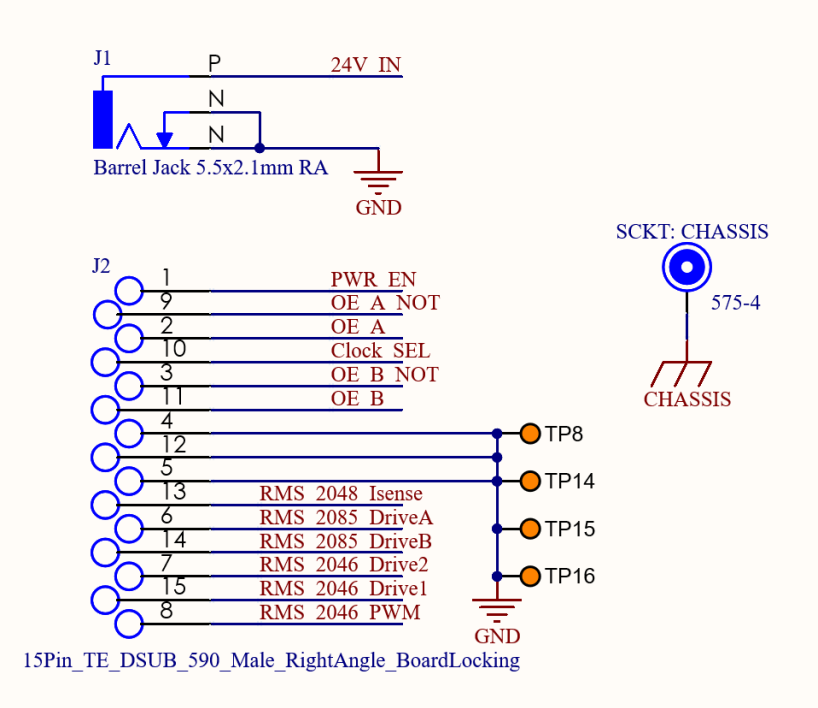

Figure 6.2. External Interfaces section of the Backbone Test Fixture schematic.

UUT Interfaces

There are three sets of electrical and mechanical interfaces on the Backbone Test Fixture. The PPUP002046 has seven #2-56 mounting holes and uses both large and small pogo pins. The large pogo pins are used for mating with larger turrets, while the small pogo pins are used for small sockets. The PPUP002048 also has seven #2-56 mounting holes, but only uses the large pogo pins. Similar to the PPUP002026 interface described in Section 5.2.1.1, the PPUP002085 uses the same pogo pins, however the PPUP002085 only has three #2-56 mounting holes.

6.2.2 Power Supply Design

±12V Power Supply

A ±12V power supply is necessary in this design to power several op-amps and RMS converters. The CUI PQMC3-D24-D12-S [30] was chosen for this design, delivering +12V @ 125mA and -12V @ 125mA. Shown in Figure 6.3 is the power supply with two load resistors present in case a minimum load needs to be set for proper regulation.

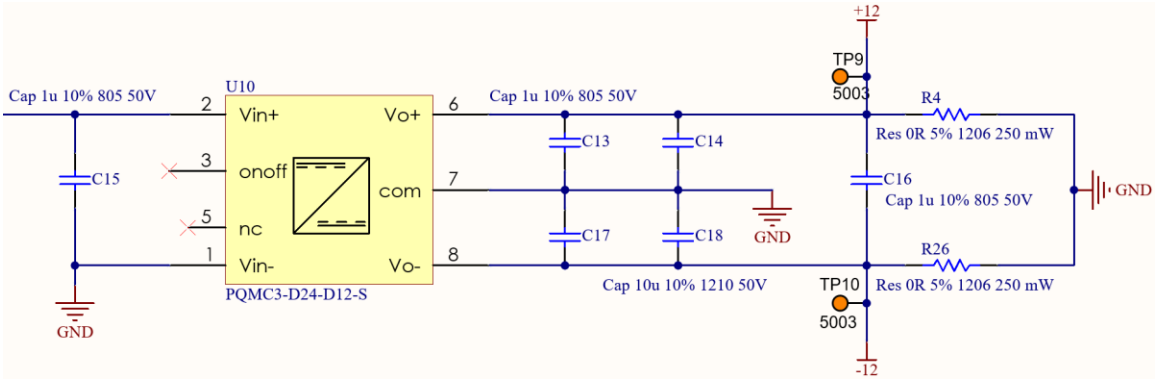

Figure 6.3. ±12V power supply section of the Backbone Test Fixture schematic, including input and output filtering.

15V Power Supply

A 15V power supply was chosen specifically for driving the gates of the MOSFETs present in the three UUTs. The CUI PQMC3-D24-S15-S [30] was chosen for this design, delivering 15V @ 200mA to the output. Shown in Figure 6.4 is the power supply with a load resistor present in case a minimum load needs to be set for proper regulation.

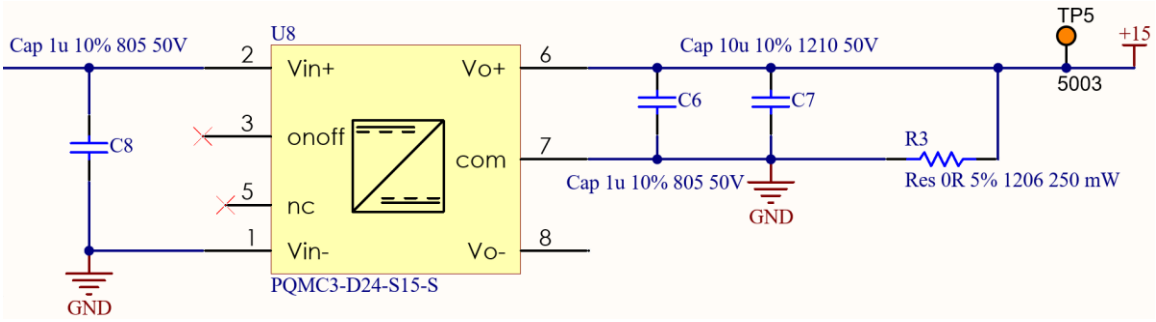

Figure 6.4. 15V power supply section of the Backbone Test Fixture schematic, including input and output filtering.

5V Power Supply

The 5V "auxiliary" supply from Section 5.2.1.1 is also used in this fixture. The 5V power supply is used for powering relays, as well as LM555 oscillators and logic buffers.

6.2.3 UUT Test Circuits

6.2.3.1 Boost and Buck Converters

For testing the PPUP002046, two boost converters and one buck converter are implemented to verify that several MOSFETs and diodes are functional. Shown in Figure 6.5 is the boost converter section of the schematic. The MOSFET used in the converter is present on the UUT. The drain of the MOSFET is connected to the "SW" node. Two

Zener diodes are added on the switching node to suppress excessive voltage spikes and prevent damage to the UUT.

Using the continuous conduction mode equations from the Texas Instruments Power Handbook [31],

$$t_1 = \frac{1}{f_{switch}} * \frac{V_{out} + V_f - V_{in}}{V_{out} + V_f} \tag{6.1}$$

$$t_2 = \frac{1}{f_{switch}} - t_1 \tag{6.2}$$

the time periods for the MOSFET being on (t_1) and off (t_2) are found. These time periods are later used in 6.2.4 to determine resistor and capacitor values for the LM555 timer.

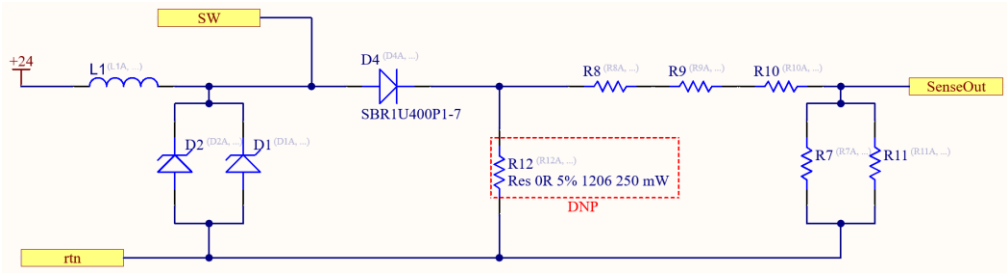

Figure 6.5. Boost converter test circuit section of the Backbone Test Fixture schematic, following the basic topology of a boost converter. The "SW" node connects to a MOSFET on the UUT. Includes a resistor divider.

Shown in Figure 6.6 is the buck converter section of the schematic. The MOSFET used in the converter is located on the UUT. The source of the MOSFET is connected to the "Buck" node. Using the continuous conduction mode equations [31],

$$t_1 = \frac{1}{f_{switch}} * \frac{V_{out} + V_f}{V_{in} + V_f} \tag{6.3}$$

$$t_2 = \frac{1}{f_{switch}} - t_1 \tag{6.4}$$

the time periods for the MOSFET being on (t_1) and off (t_2) are found. These time periods are later used in 6.2.4 to determine resistor and capacitor values for the LM555 timer.

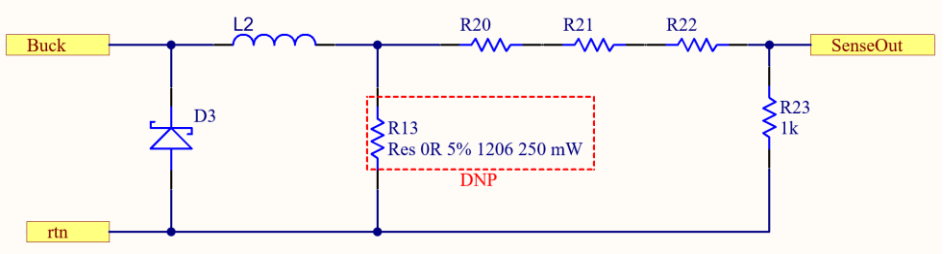

Figure 6.6. Buck converter test circuit section of the Backbone Test Fixture schematic, following the basic topology of a buck converter. The “Buck” node connects to a MOSFET on the UUT. Includes a resistor divider.

6.2.3.2 Push-Pull Converter

The objective of the push-pull converter is to verify that two MOSFETs and two diodes on the PPUP002048 are functioning. Shown in Figure 6.7 is the push-pull converter section of the schematic.

The X701 and X703 nets are connected to two MOSFETs. The X704 and X705 nets are connected to two diodes. By switching the MOSFETs, a current is applied to both diodes on the opposite side of the transformer. The current passed through these diodes is measured at the X706 net via a current sense amplifier. The details of this amplifier are discussed later in the chapter.

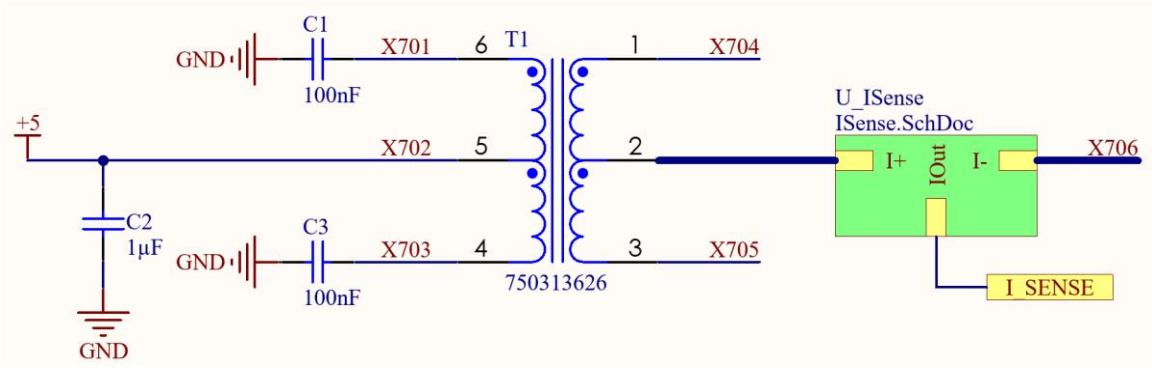

Figure 6.7. Push-pull converter test circuit section of the Backbone Test Fixture schematic, including a transformer, connections to the UUT, and current sense amplifier sub-circuit.

6.2.3.3 Capacitor Divider

To test the outputs of the PPUP002085, a capacitor divider was implemented. Since the outputs of the PPUP002085 are typically for driving the gates of MOSFETs, having a representative load was key, as a capacitor divider can simulate the load of a MOSFET gate. The circuit for the capacitor divider is shown in Figure 6.8. This circuit has been verified to function on the previous version of the Backbone Test Fixture at Orbion and is retained in the design.

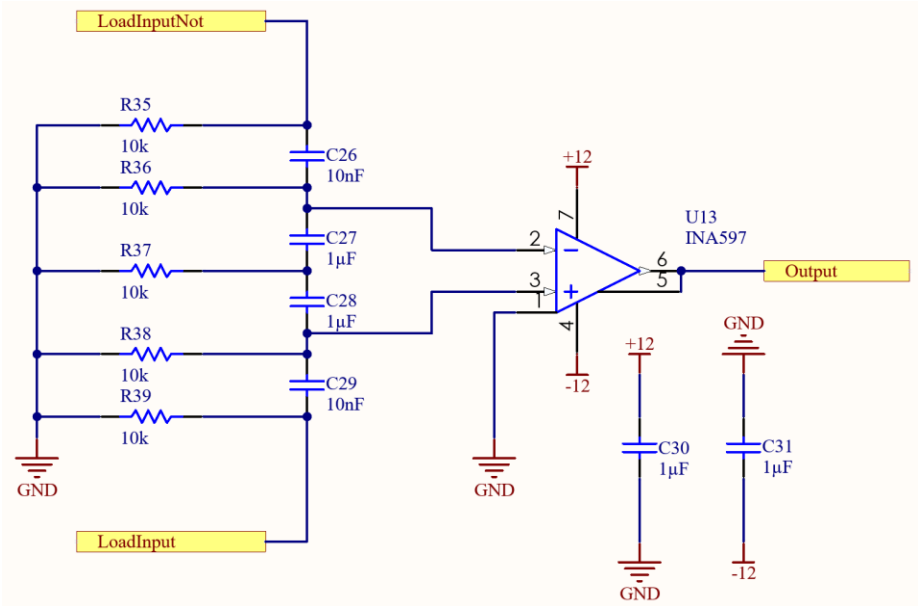

Figure 6.8. Capacitor divider section of the Backbone Test Fixture schematic, including the capacitive divider and difference amplifier.

6.2.4 MOSFET Timing and Drive Circuits

Due to the designs of the three UUTs, oscillators are necessary. The MOSFETs on the PPUP002046 and PPUP002048 are driven by two clock signals in the PPU. These two clock signals are 180 degrees out of phase from each other.

To generate the two clock signals on this test fixture, FOD3150V opto-coupled gate driver ICs [32] are utilized. For the in-phase clock signal, the input is connected to the anode of the driver LED. For the out-of-phase clock signal, the input is connected to the cathode of a second FOD3150V. When the clock is HIGH, the anode-connected diode will conduct, enabling the output, while the cathode-connected diode will not conduct, keeping the output disabled. When the clock is LOW, the opposite will occur, generating the 180 degree phase difference.

Four clocks (two in-phase, two out-of-phase) are designed into the Backbone Test Fixture, however, only two will be active at a time for a given test case. To control which of the four clocks are active and buffer the input clock signals, four 74LVC1G126 buffers [33] are used. The output enable pins on the buffers are controlled from the external DSUB interface. Buffering the clock signals is also necessary to generate the out-of-phase clocks, as one buffer must source power and another buffer must sink the power for each diode in the FOD3150V. The buffer and gate drive circuitry are shown on the right side of Figure 6.9.

To drive the four buffers, two LM555 [34] oscillators are designed in the schematic. Two oscillators are necessary as the UUTs require two different frequencies and duty cycles, depending on which UUT is being tested. Each LM555 oscillator is configured as an

astable timer, with two resistors and a capacitor required to set the frequency and duty cycle. By selecting the resistor and capacitor values and using the equations

$$T_h = 0.693 * (R_1 + R_2) * C_1 \tag{6.5}$$

$$T_l = 0.693 * R_2 * C_1 \tag{6.6}$$

$$f = \frac{1.44}{(R_1 + 2R_2) * C_1} \tag{6.7}$$

from the LM555 datasheet, the time-high T_h, time-low T_l, and frequency f of each oscillator were found. The time-high and time-low values aligned with those found in for the boost and buck converters in 6.2.3.1. The two LM555 oscillator circuits are shown on the left side of Figure 6.9.

Lastly, a method of switching between the two oscillators is required. The switching is accomplished using the Relay Sub-Circuit with the oscillators connected to different inputs. The clock output is connected to the normally closed of input A, and the normally-open of input B. By actuating the Clock_SEL signal from the external interface, the two oscillators can be switched.

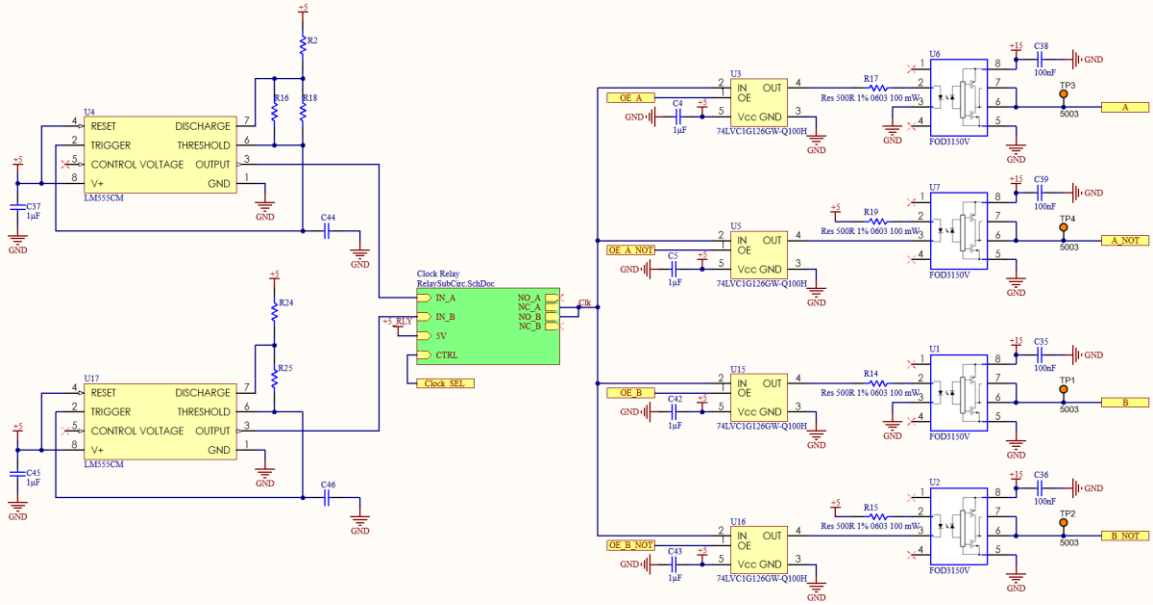

Figure 6.9. Clock Drive section of the Backbone Test Fixture schematic, including two LM555 oscillators, relay sub-circuit switch, logic buffers, and MOSFET drivers.

6.2.5 Current Sense Amplifier

To sense the current returned to the transformer in the push-pull converter, a current sense op-amp circuit was designed. The circuit for the current sense amplifier is shown in Figure 6.10. The return current is passed through R44, and the voltage drop is measured

across U14A. U14B amplifies the output then passes the signal through a high-pass-filter capacitor. This circuit has been verified to function on the previous version of the Backbone Test Fixture at Orbion and is retained in the design.

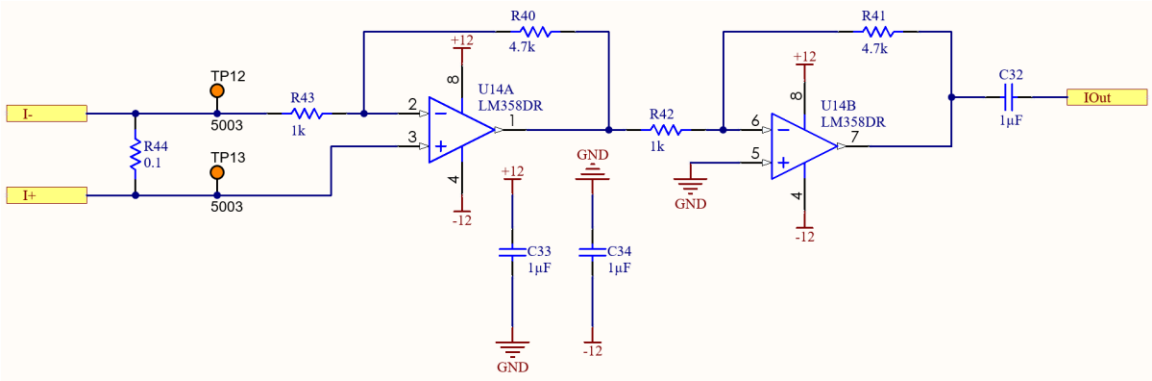

Figure 6.10. Current sense amplifier section of the Backbone Test Fixture schematic, including a sense resistor and two operational amplifiers.

6.2.6 RMS to DC Converter

In the design of the Backbone Test Fixture, a total of six AC voltage measurements are conducted. These six measurements need to be output to the external interface for a DAQ to read. However, the Nyquist frequency of the AC measurements is well above the maximum sampling rate of a DAQ system such as the USB-6002. In order to use the same DAQ hardware across both test fixtures, an analog conversion needs to occur on the test fixture before outputting the voltage to the DAQ.

To perform this analog conversion, the Analog Devices AD737 True RMS-to-DC Converter [35] was selected. This IC performs a true Root Mean Square (RMS) calculation, calculating the equivalent DC voltage for an AC waveform . The DC voltage can easily be sampled by the DAQ, as there is now no AC component. The output of the AD737 is scaled between 0V and 200mV, so the U12 circuit amplifies the output up to the DAQ maximum input voltage of 10V. This circuit has been verified to function on the initial version of the Backbone Test Fixture and has been kept in the design.

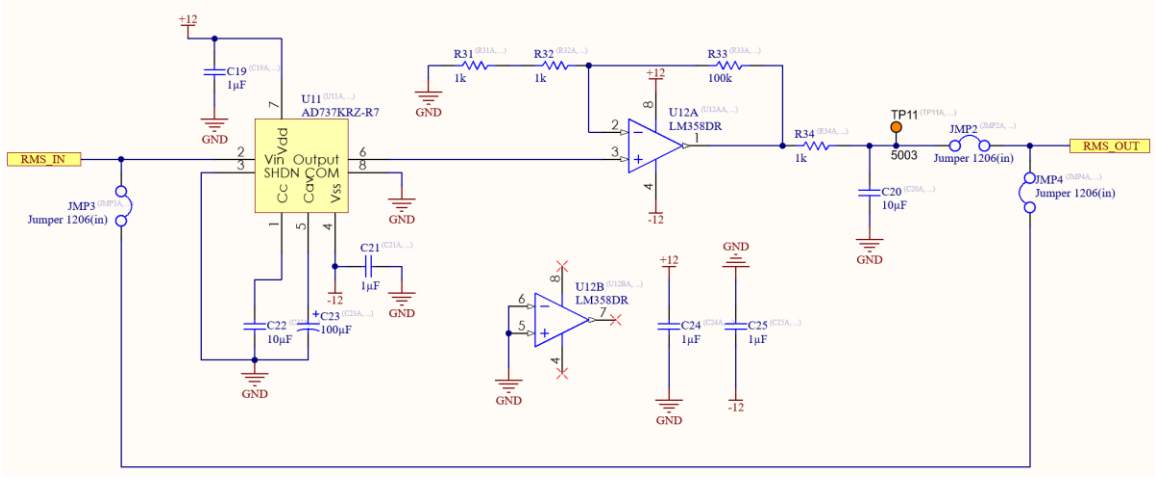

Figure 6.11. RMS to DC conversion section of the Backbone Test Fixture schematic, including the AD373 and a signal amplifier.

6.3 Conclusion & Future Work

At the time of writing this report, the Backbone Test Fixture PCBA design is approved and released at Orbion Space Technology. The PCBA will be procured and functionally verified. In the future, additional elements such as the electrical harness and software will be designed and verified as well.

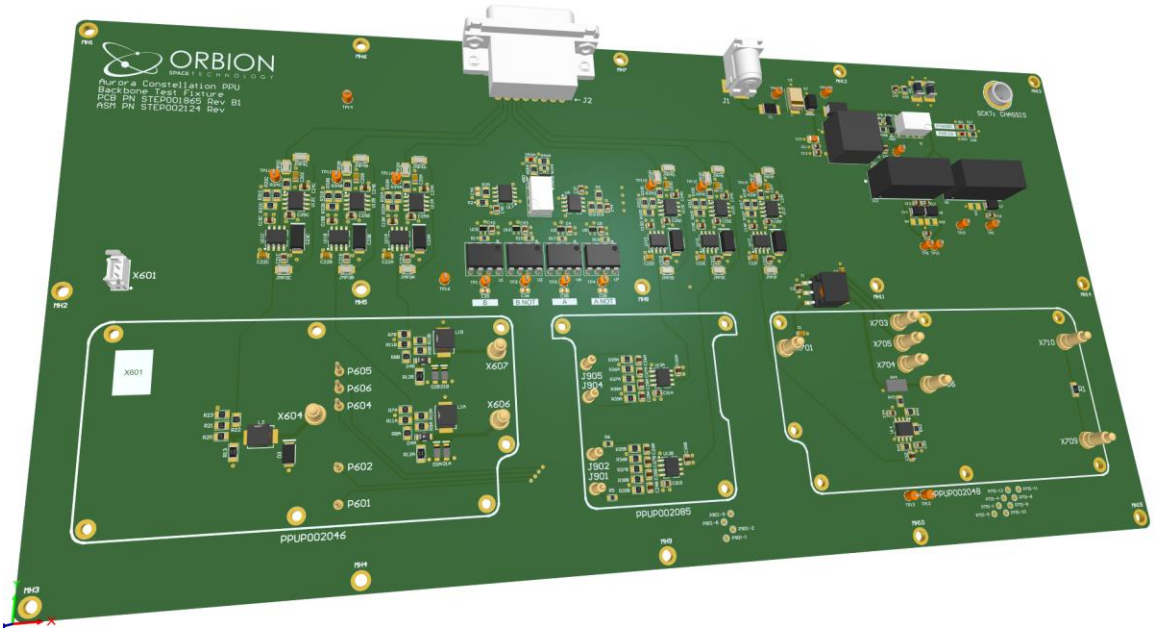

Figure 6.12. Backbone Test Fixture PCBA 3D model.

7 Conclusions

In this project, three designs were developed following the requirements and methods from Chapters 2 and 3: a 200V DC-DC converter, a test fixture for the PPUP002026, and a test fixture for the PPUP002046, PPUP002048, and PPUP002085.

The revision B1 of the 200V DC-DC Converter conformed to all IPC requirements defined in Chapter 2. The design process was extensive due to the from-scratch iterative design approach: simulating the circuit in LTspice, modifying an evaluation board to prototype the design, and then manufacturing two revisions of the Orbion PCBA. While extensive, the design process was crucial for fully understanding the nuances and performance of the LT8304-1 controller IC. As the revision B1 design conformed to all requirements, the 200V DC-DC converter was utilized in the PPUP002026 test fixture.

The PPUP002026 Test Fixture was successfully designed and verified to all design and performance requirements specified in Chapter 2. The fixture PCBA interfaced electrically and mechanically without damaging the PPUP002026, functioned off a single 24V power supply, utilized automotive qualified parts where possible, and implemented representative electrical loads for the PPUP002026. The PCBA only had one anomaly, which was resolved by replacing one component with a higher rated part. The automated testing software successfully controlled the relays present on the fixture and output the correct signals to the PPUP002026. The software was verified to catch anomalies during testing a UUT and featured a functional and informative user interface for the operator. Due to the successful verification, the test fixture is ready to be used for performing functional tests with the PPUP002026 hardware, however only in a lab environment until the FMEA and manufacturing qualification is completed.

The Backbone Test Fixture, designed for testing the PPUP002046, PPUP002048, and PPUP002085, conformed to the design requirements outlined in Chapter 2. The fixture PCBA is designed to electrically and mechanically interface with the three UUTs, function off a single 24V power supply, and test the UUTs in a representative flight-like manner. Several test circuits to perform the functional testing were also developed: an oscillating timing circuit, boost/buck/push-pull converters, and a RMS to DC conversion circuit. Other sections of the fixture design, such as the capacitor divider and current sense amplifier, are verified past working designs from the previous version of the fixture. In the future, the Backbone Test Fixture PCBA will be manufactured, the DAQ system and harness will be designed and manufactured, and the automated software will also be designed. All three key components will then be verified in the same manner as the PPUP002026 test fixture.

In conclusion, the 200V converter and two test fixtures presented in this project are key to the functional testing effort of the PCBAs in the Auora HET system PPU and can be qualified and utilized for the manufacturing environment.

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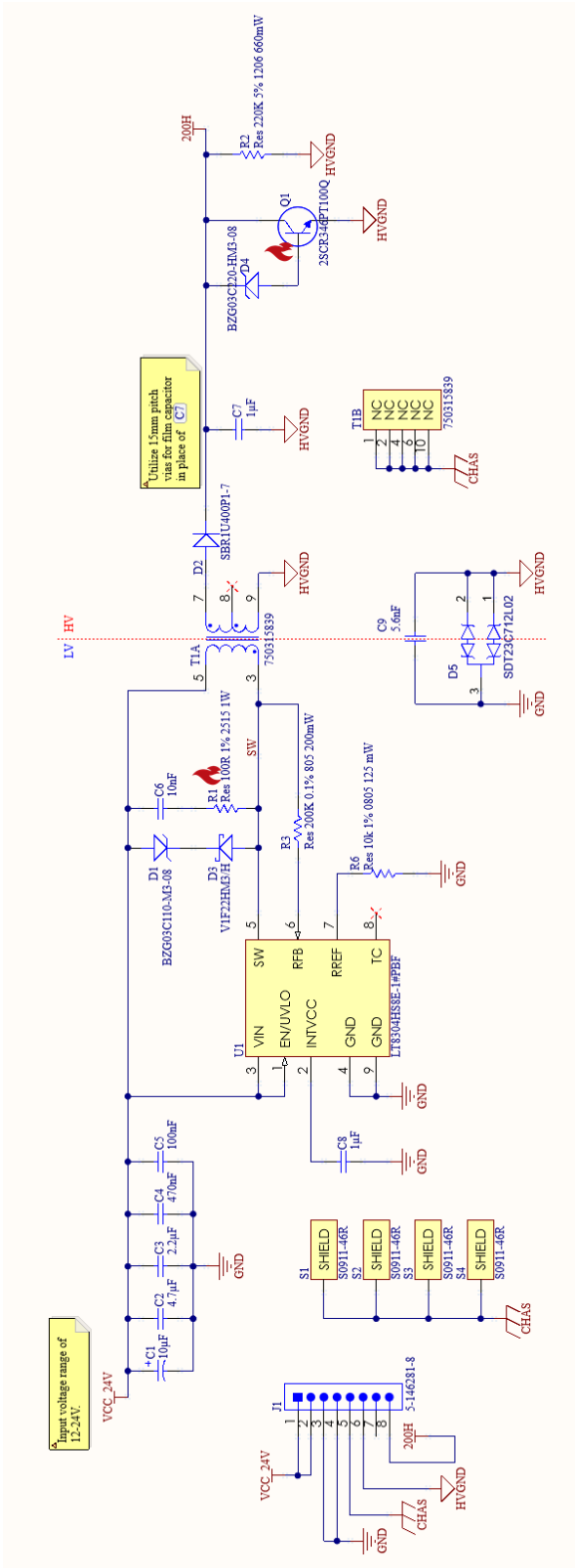
A 200V DC-DC Converter Schematic



B PPUP002026 Test Fixture Harness Drawing