9-1-2024

Design and Analysis of Self-Tanked Stepwise Charging Circuit for Four-Phase Adiabatic Logic

William Morell
LSU College of Engineering

Jin Woo Choi
Michigan Technological University, choijw@mtu.edu

Follow this and additional works at: https://digitalcommons.mtu.edu/michigantech-p2

Part of the Electrical and Computer Engineering Commons

Journal of
Low Power Electronics and Applications

MDPI

Article

Design and Analysis of Self-Tanked Stepwise Charging Circuit for Four-Phase Adiabatic Logic

William Morell [1,*] and Jin-Woo Choi [2]

[1] School of Electrical Engineering and Computer Science, Louisiana State University, Baton Rouge, LA 70803, USA
[2] Department of Electrical and Computer Engineering, Michigan Technological University, Houghton, MI 49931, USA; choijw@mtu.edu
* Correspondence: wmorel3@lsu.edu

Abstract: Adiabatic logic has been proposed as a method for drastically reducing power consumption in specialized low-power circuits. They often require specialized clock drivers that also function as the main power supply, in contrast to standard CMOS logic, and these power clocks are often a point of difficulty in the design process. A novel, stepwise charging driver circuit for four-phase adiabatic logic is proposed and validated through a simulation study. The proposed circuit consists of two identical driver circuits each driving two opposite adiabatic logic phases. Its performance relative to ideal step-charging and a standard CMOS across mismatched phase loads is analyzed, and new best practices are established. It is compared to a reference circuit consisting of one driver circuit for each phase along with a paired on-chip tank capacitor. The proposed driver uses opposite logic phases to act as the tank capacitor for each other in a "self-tanked" fashion. Each circuit was simulated in 15 nm FinFET across a variety of frequencies for an arbitrary logic operation. Both circuits showed comparable power consumption at all frequencies tested, yet the proposed driver uses fewer transistors and control signals and eliminates the explicit tank capacitors entirely, vastly reducing circuit area, complexity, and development time.

Keywords: adiabatic logic; stepwise charging; tank capacitor; FinFET

check for updates

Citation: Morell, W.; Choi, J.-W. Design and Analysis of Self-Tanked Stepwise Charging Circuit for Four-Phase Adiabatic Logic. *J. Low Power Electron. Appl.* **2024**, *14*, 34. https://doi.org/10.3390/jlpea14030034

Academic Editor: Orazio Aiello

Received: 3 March 2024
Revised: 17 June 2024
Accepted: 24 June 2024
Published: 27 June 2024

1. Introduction

Adiabatic logic, a novel approach in low-power digital circuit design, has been proposed as a method to increase the energy efficiency of digital circuits, especially in energy constrained applications such as IoT devices and other embedded systems. By employing adiabatic logic, these energy-constrained applications can achieve notable improvements in energy efficiency, allowing for prolonged battery life, reduced power consumption, and enhanced overall performance. The main principle by which an adiabatic logic circuit differs from a typical CMOS logic circuit lies in the differing methods of charging or discharging a load capacitance in the system through careful control of the power supply [1]. By smoothly ramping between different target voltages (i.e., a logic high or a logic low), losses caused by charging the load capacitance of each logic gate can be reduced. Often, this can require complex resonant circuits adding to design time and reducing manufacturability [2–5]. Alternatively, stepwise charging can be used to find a middle ground between typical CMOS logic power consumption and ideal adiabatic logic operation [6–10]. Instead of smoothly transitioning between targets as in ideal adiabatic logic or sharply jumping between a logic high and a logic low, step-charging transitions between multiple intermediate voltage levels. Step-charging energy consumption approaches that of ideal adiabatic charging as the number of steps increases. These step-charging circuits can require multiple supply voltage levels or large on-chip tank capacitors in their design. This work aims to reduce design time and chip area by use of a redesigned step-charging driver circuit that eliminates the need for tank capacitors.

2. Adiabatic Logic

Consider a typical CMOS inverter with a load capacitance C as shown in Figure 1. During a charging event, an amount of charge $Q = CV_{DD}$ travels from the power supply to the load capacitance through the pull-up PFET. Now, the voltage across the load is equal to the supply voltage V_{DD} and the capacitor stores an amount of energy $E_{stored} = \frac{1}{2}CV_{DD}^2$, but an amount of energy equal to $E_{total} = QV_{DD} = CV_{DD}^2$ leaves the power supply. The difference is lost in the upper transistor (PFET). Similarly, it can be easily seen that during a discharging event, all the charge stored in the capacitor is dumped to ground through the lower transistor (NFET), and all the stored energy is lost in the NFET. Charging and discharging events both consume an amount of energy, $E_{lost} = \frac{1}{2}CV_{DD}^2$, regardless of any properties of the NFETs or PFETs that comprise the logic gates.

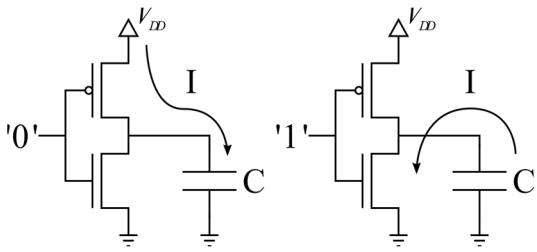


Figure 1. CMOS inverter circuit showing the current path during both a charging and discharging event. The capacitor C represents the load created by attaching further logic gates to the inverter.

By contrast, during adiabatic charging of the same system, the supply voltage, v_S, is not static but slowly ramps from 0 V to V_{DD} over a time T. In doing so, the voltage across the load capacitance can be modeled as approximately following the supply voltage, that is, $v_C \approx v_S = \frac{V_{DD}}{T}t$. In doing so, the overall energy dissipated in charging the capacitor over this time period can be found:

$$E_{lost} = \frac{RC}{T}CV_{DD}^2 \tag{1}$$

where R is the on-resistance of the PFET PMOS channel during charging. Through this method, less than $\frac{1}{2}CV_{DD}^2$ energy can be lost during a charging event through careful control of device parameters and charging time.

There is a variety of circuit architectures that implement this adiabatic charging method, with a common application being in different four-phase adiabatic logic families such as "efficient charge recovery logic" (ECRL) [11] and "positive feedback adiabatic logic" (PFAL) [12]. In both families, the ideal power supply consists of a trapezoidal power clock, as illustrated in Figure 2a. Four separate phases occur in the power clock: evaluate, hold, recover, and wait. During the evaluate phase, the supply voltage follows the ramp illustrated earlier and allows for the logic gate to perform its computation. The hold phase holds the output logic values for any successor logic to evaluate its own operation. Recover allows for the charge in the load capacitance to return to the power supply and the wait phase provides symmetry for smooth operation. Four different power clocks are required to implement an ECRL or PFAL system, staggered as shown in Figure 2b, with the evaluate phase being in line with its predecessor's hold phase. Logic is thus chained together as in Figure 3, with each gate passing data along in a pipeline.

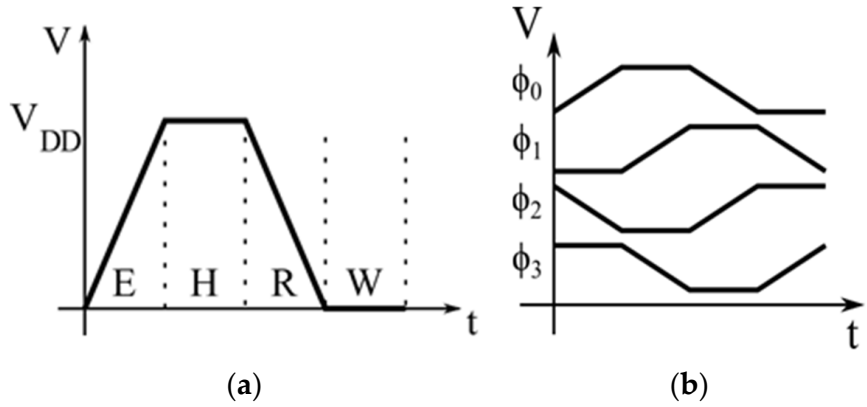


Figure 2. Ideal trapezoidal power clocks for adiabatic logic. (**a**) Power clock showing relative voltage levels during each phase of operation: evaluate, hold, recover, and wait; (**b**) four staggered power clocks used in four-phase adiabatic logic, each offset 90 degrees such that the evaluate phase of one clock is during the hold phase of its predecessor.

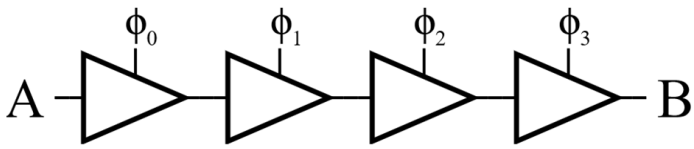


Figure 3. Four successive buffers implemented in four-phase adiabatic logic, buffering a logical value from point A to B, each taking a different power clock in sequence.

3. Stepwise Charging

As mentioned previously, for PFAL and ECRL, generation of the ideal trapezoidal waveform is quite difficult and can require carefully tuned resonant circuits. To this end, alternative methods consisting of multiple steps to intermediate voltages in the charging process to mimic the smooth ramp up have been investigated [6–10]. The simplest of these is the two-step charging case illustrated in Figure 4. A switch brings the load capacitance to half the supply voltage during the evaluation phase, dissipating $\frac{1}{8}C_L V_{DD}^2$, followed by a second switch to V_{DD} and dissipating another $\frac{1}{8}C_L V_{DD}^2$. While nowhere near as efficient as the ideal trapezoidal behavior in (1), the two-step case results in only $\frac{1}{4}C_L V_{DD}^2$ being lost in each charge or discharge cycle, half that of conventional CMOS.

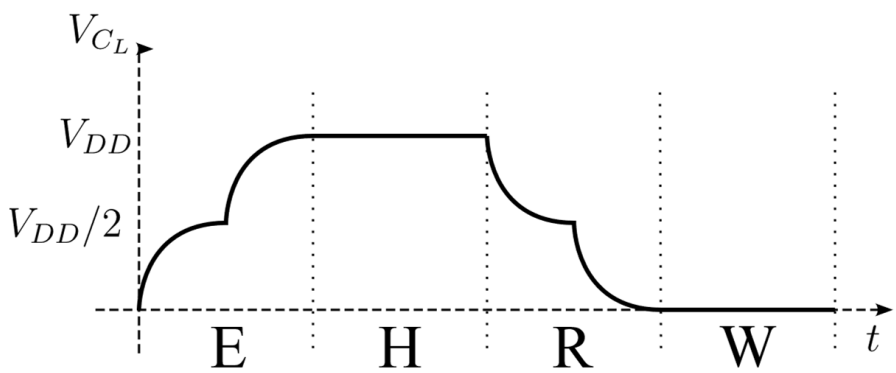
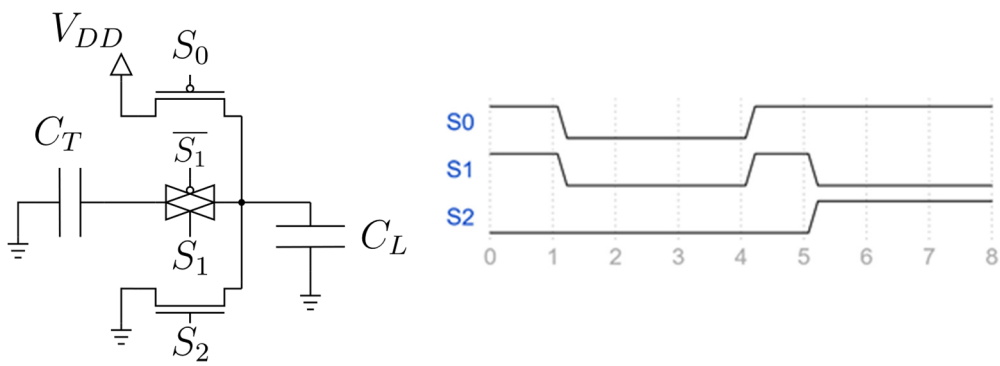


Figure 4. Stepwise charging of a load capacitance using two steps, each contributing half the charge needed to reach supply voltage. The four phases used in this clock match those of the trapezoidal clock of Figure 2a. The exponential behavior of charging and discharging the load capacitance is exaggerated for illustration.

To implement step-charging, specific driver circuits are used, as demonstrated in [7] and shown in Figure 5a. These consist of a large tank capacitance C_T and pass-transistors for moving the required charge around. This driver circuit is controlled by a finite state machine of conventional CMOS logic with an operating frequency higher than that of the driven adiabatic logic (with the goal that the power saved by using adiabatic logic is not outweighed by the power consumed by the driver circuit and control logic). During the beginning of the evaluate and recover phases of the power clock the transmission gate controlled by S_1 levels the voltage between C_L and C_T, ideally bringing both their voltages to $\frac{V_{DD}}{2}$. During the latter half of these phases, either S_0 or S_2 drives C_L to the supply voltage or ground, respectively. The control signal timing for the step driver can be seen in Figure 5b.



(**a**) (**b**)

Figure 5. Traditional stepwise charging driver circuit. (**a**) The driver circuit; different pass transistors control the flow of charge to the power clock node represented by capacitor C_L. The tank capacitor C_T sources or sinks charge during the middle of evaluate and recover phases, respectively. (**b**) Control signal timing for each of the pass transistors.

One of these driver circuits and companion FSM is required for each power clock and the tank capacitance must be tuned to match the load carried by that specific clock's logic, with a larger tank capacitance allowing the step voltage to be closer to half the supply, improving efficiency, though with more area overhead. In [7], it was found that a tank capacitance equal to ten times the load capacitance was a good rule of thumb for proper logical operation and circuit efficiency before hitting diminishing returns. In practice, this requires careful investigation of the load represented by each phase of logic and an additional area overhead needed to implement the large tank capacitance. A total of 4 tank capacitances, 12 switching devices, and 12 different control signals are thus required to implement this system for any four-phase adiabatic logic.

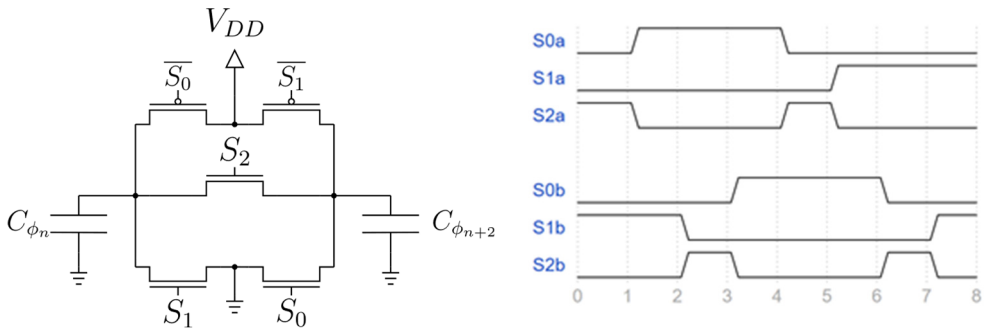
4. Improved Step-Charging Circuit

An improved step-charging circuit can be implemented using the circuit shown in Figure 6a. In contrast to the reference work, only two of these circuits are needed, one for each pair of opposite logic phases. Thus, only 10 switching devices and control signals are required, and importantly, no explicit tank capacitors are required. It achieves this by using the load capacitance, C_n, of phase ϕ_n as the tank capacitor for its opposite phase ϕ_{n+2} and vice versa in a "self-tanked" fashion.

When one phase is dropping in its first step down from V_{DD}, this charge is used to step up the opposite phase from ground. If the load capacitances for each phase are equal, then any charge will be distributed equally, the step voltage will be equal to $\frac{V_{DD}}{2}$, and the energy consumed remains at half of that of a conventional CMOS. If the load capacitances are not equal (a more likely scenario), then the load capacitances for each phase can be defined as such: C_L is the nominal CMOS load and will correspond to the phase with the lower load and C_H will correspond to the phase with the higher load. $C_H = \alpha C_L$ and

$\alpha \geq 1$, α representing the factor by which one phase's load is larger than the other. Note that the order of these two loads does not matter, as a full cycle of their power clocks will be considered. Due to charge conservation between the mismatched capacitances, two different step voltages occur at different points in the power clock:

$$V_{step-A} = \frac{1}{\alpha+1} V_{DD} \qquad and \qquad V_{step-B} = \frac{\alpha}{\alpha+1} V_{DD} \tag{2}$$



(**a**) (**b**)

Figure 6. Improved stepwise charging driver circuit. (**a**) The driver circuit; different pass transistors control the flow of charge between to opposite phases of the adiabatic logic, represented here by their loads and relative offset from each other: C_{ϕ_n} and $C_{\phi_{n+2}}$; (**b**) Control signal timing for each of the pass transistors, separated into 'a' control signals for ϕ_0 and ϕ_2, and 'b' signals for ϕ_1 and ϕ_3.

ϕ_L, the clock corresponding to the lower load, will attain $\frac{\alpha}{\alpha+1} V_{DD}$ on its way to charging to V_{DD}, while lowering to $\frac{1}{\alpha+1} V_{DD}$ on its descent to 0 V. ϕ_H will do just the opposite on its way up and down. Now, a charging event and the energy lost for ϕ_L can be decomposed into its two steps:

$$E_{L,charging} = \frac{1}{2} C_L \left(\frac{\alpha}{\alpha+1} V_{DD} \right)^2 + \frac{1}{2} C_L \left(V_{DD} - \frac{\alpha}{\alpha+1} V_{DD} \right)^2 \tag{3}$$

$$E_{L,charging} = \frac{1}{2} C_L V_{DD}^2 \left[1 - 2\frac{\alpha}{\alpha+1} + 2\left(\frac{\alpha}{\alpha+1} \right)^2 \right]. \tag{4}$$

A discharge event and its energy can be decomposed in the same way:

$$E_{L,discharging} = \frac{1}{2} C_L V_{DD}^2 \left[1 - 2\frac{1}{\alpha+1} + 2\left(\frac{1}{\alpha+1} \right)^2 \right]. \tag{5}$$

Combined, the overall energy lost during a complete cycle of ϕ_L can be shown as follows:

$$E_L = \frac{1}{2} C_L V_{DD}^2 \cdot 2\frac{\alpha^2+1}{(\alpha+1)^2}. \tag{6}$$

It is at this moment that two interesting observations can be made. Setting $\alpha = 1$, results in the case with no mismatch and an overall energy loss of $\frac{1}{2} C_L V_{DD}^2$ for both a single charge and discharge, congruent with the results stated in the goals of stepwise charging (note that $E_{CMOS} = C_L V_{DD}^2$ when combining a single charge and discharge). Additionally, taking the limit as $\alpha \to \infty$ results in $E_L = C_L V_{DD}^2$, again, the standard CMOS result. This factor can be thought of as corresponding to a higher load capacitance whose voltage cannot be changed no matter how much charge is taken out of it, a $V_{step-A} = 0\ V$, and a $V_{step-B} = V_{DD}$. Thus, the higher capacitance acts as a static voltage source, just like a CMOS power supply.

The same process of finding energy loss can be performed for C_H as well, remembering to factor in α for the load capacitance being a higher value, resulting in the following:

$$E_H = \frac{1}{2} C_L V_{DD}^2 \cdot 2\alpha \frac{\alpha^2 + 1}{(\alpha + 1)^2}. \tag{7}$$

Again, this can be checked for congruence to the no mismatch case by setting $\alpha = 1$, and indeed does result in half the energy of standard CMOS charging. Combining both (6) and (7), a combined energy loss for the two mismatched phases can be determined:

$$E_H + E_L = C_L V_{DD}^2 \cdot \left[\alpha \frac{\alpha^2 + 1}{(\alpha + 1)^2} + \frac{\alpha^2 + 1}{(\alpha + 1)^2} \right] = C_L V_{DD}^2 \left[\frac{\alpha^2 + 1}{\alpha + 1} \right]. \tag{8}$$

Similarly, the energy for a standard CMOS circuit going through both a charge and discharge cycle with two different loads can also be determined:

$$E_{CMOS} = E_{H,CMOS} + E_{L,CMOS} = \alpha C_L V_{DD}^2 + C_L V_{DD}^2 = (\alpha + 1) C_L V_{DD}^2. \tag{9}$$

An energy savings factor can then be defined as the ratio between (8) and (9):

$$ESF\% = \frac{E_H + E_L}{E_{H,CMOS} + E_{L,CMOS}} = \frac{\alpha^2 + 1}{(\alpha + 1)^2}. \tag{10}$$

For the matched $\alpha = 1$ case, this again shows that the step-charging circuit will use half the energy of a standard CMOS circuit. Even if the higher load in a phase is twice that of the lower, this still results in an energy consumption 55% that of standard CMOS.

It may seem prudent at this point to add additional compensation capacitance to the lower load phase to force $C_H = C_L$ and $\alpha = 1$. However, doing so changes the combined energy of the step-charging phases to the following:

$$E_{H,compensated} + E_{L,compensated} = \alpha C_L V_{DD}^2. \tag{11}$$

This can be compared to the unadjusted energy in (8) to determine how much compensation adjusts the energy used:

$$Compensation\ \%\ Change = \frac{E_{H,compensated} + E_{L,compensated}}{E_H + E_L} = \frac{\alpha^2 + \alpha}{\alpha^2 + 1}. \tag{12}$$

For $\alpha > 1$, this always results in more energy being used in the compensated case vs. the uncompensated case in (10). Therefore, there is no benefit to adding capacitance to the lower load to account for a mismatch between phases.

5. Implementation and Simulation

A test circuit was designed using the FreePDK15 15 nm FinFET PDK provided by North Carolina State University [13].

This circuit consisted of two of the step-charging driver circuits depicted in Figure 6a as well as an example test logic circuit (Figure 7) implemented in ECRL using the methods laid out in [11]. Buffers were interspersed to add additional load to the example circuit as well as to keep signals properly in-phase as they are pipelined through the circuit in accordance with ECRL design principles. Control signals for the step-driver circuits were defined using idealized voltage sources and follow the timing of Figure 6b.

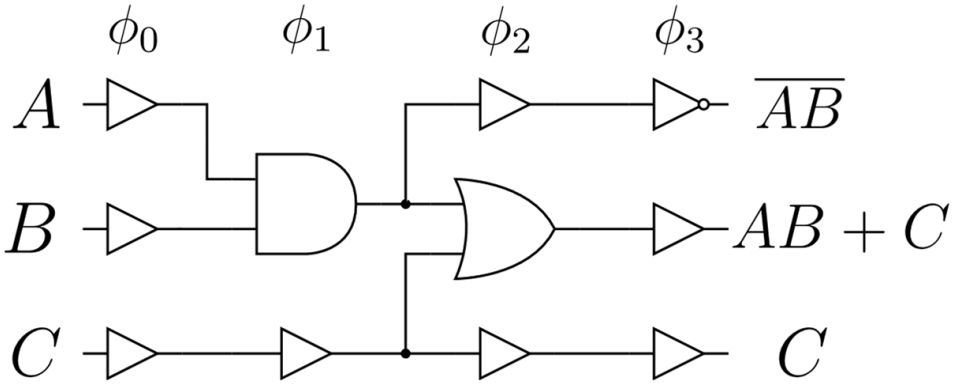


Figure 7. Logic circuit used to test the power consumption of the stepwise charging driver circuits. Each combination of logic signals A, B, and C were tested. Each gate was implemented in ECRL, and buffers were included to ensure proper timing of signal propagation through the circuit. Each logic gate used minimized FinFETs as allowed for by the PDK with two fins per device.

All FinFETs used in the simulation were of minimum sizing, as detailed in the PDK with two fins used per device. V_{DD} was set to 0.8 V.

The A, B, and C data signals depicted in Figure 7 merely count up from a binary 0 with A being the least significant bit and C being the most significant, allowing for all logical results to be evaluated for the average power consumption. All results are available after one ECRL period after being applied due to the inherent pipelining of ECRL.

The proposed system was compared to the reference driver circuit in Figure 5. First an implementation of the reference driver circuit was designed using minimum sized FinFET parameters and two fins per device. Control signals were also created using ideal voltage sources. This is to keep consistency with the proposed driver implementation. Then, a sweep of the tank capacitor for each driver was performed to confirm the findings laid out in [7], each of the four drivers receiving identical capacitance values. The reference drivers were attached to each clock phase for the test logic circuit and driven to result in an adiabatic logic frequency of 250 MHz. Average power consumption was then computed for these simulations. These results can be seen in Figure 8. After a tank capacitance of 20 fF, savings in power suffers from significant diminishing returns. Therefore, 20 fF was chosen as the baseline for tank capacitor in the reference driver circuit, with 100 fF being used as an extreme to compare efficiency with the proposed driver circuit. In all reference driver simulations, tank capacitors were pre-charged to 0.4 V in order to model the circuit having reach its steady state of operation, with the goal being to mimic the "few cycles to settle" requirement laid out in [7]. Simulations for each circuit were then performed at a range of adiabatic system frequencies (100 MHz to 1 GHz), and power consumption for each system (proposed, reference at 20 fF, and reference at 100 fF) was calculated.

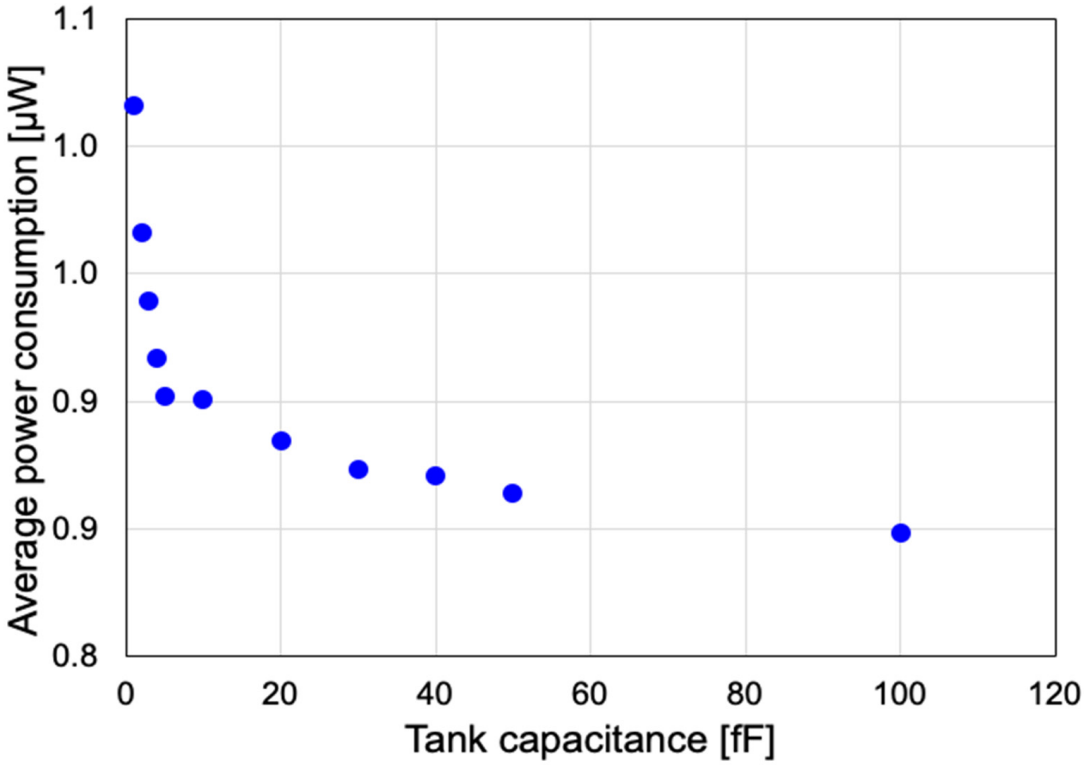


Figure 8. Tank capacitor sweep at 250 MHz operation of the reference driver and test logic circuit. After about 20 fF of tank capacitance on each phase, the circuit hits diminishing returns in regard to power savings.

6. Analysis

All test logic circuits adequately performed the logical operations required under their respective drivers, confirming that both methods are sufficient for proper logical operation. Power consumption across the frequency range for each driver is shown in Figure 9. As can be seen, across the majority of the frequency range, both the 20 fF reference driver, the 100 fF reference driver, and the proposed driver perform within 1% of each other with regard to power consumption. Lower frequencies slightly deviate from each other as these ranges are more dominated by leakage power rather than the dynamic switching power. Additionally, when observing the waveforms of the clocks in Figure 10 for the proposed driver, the mismatch in load between the phases can be seen. ϕ_0 and ϕ_2 are relatively well balanced, and their step voltages do not deviate far from $\frac{V_{DD}}{2}$ during either charging or discharging. This can be explained by the relatively even load for each phase based on the logic used in Figure 7. ϕ_1 and ϕ_3, however, show a deviation to about 480 mV at the worst in a given charge or discharge cycle. Again, by looking at Figure 7, it is easy to see that the load seen by ϕ_3 is the lowest in the circuit, as the outputs of logic gates driven by ϕ_3 do not drive any other gates, only their self-loading is present. Adding dummy load to clock 3 in the form of capacitor connected NFETs allowed for the step voltage to reach closer to the ideal of $\frac{V_{DD}}{2}$, in agreement with (2) and the reduction in α to be closer to 1, but overall increased the power consumed by the circuit in agreement with the findings in (11) and (12).

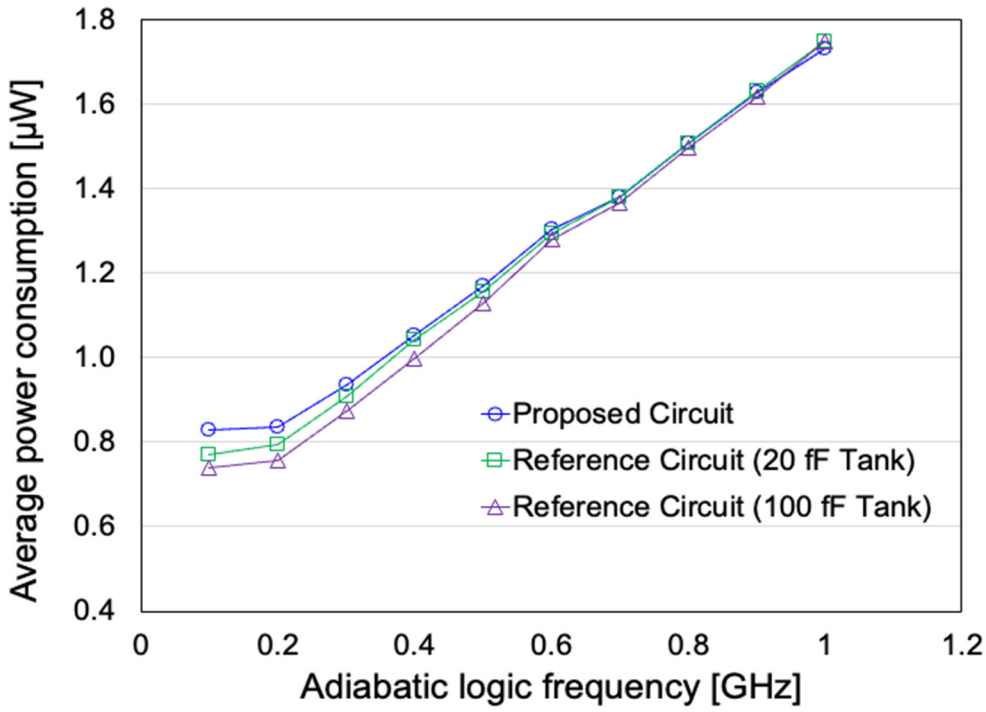


Figure 9. Comparison of power consumption for each circuit under test at different adiabatic logic frequencies. The proposed stepwise charging driver circuit is compared to the reference work at with both 20 fF and 100 fF tank capacitors. During low-frequency operation, power is largely dominated by leakage current and little change in power consumption occurs with a change in frequency. As frequency increases, power scales linearly. Higher frequencies show power consumptions within 1% of each other for each circuit under test.

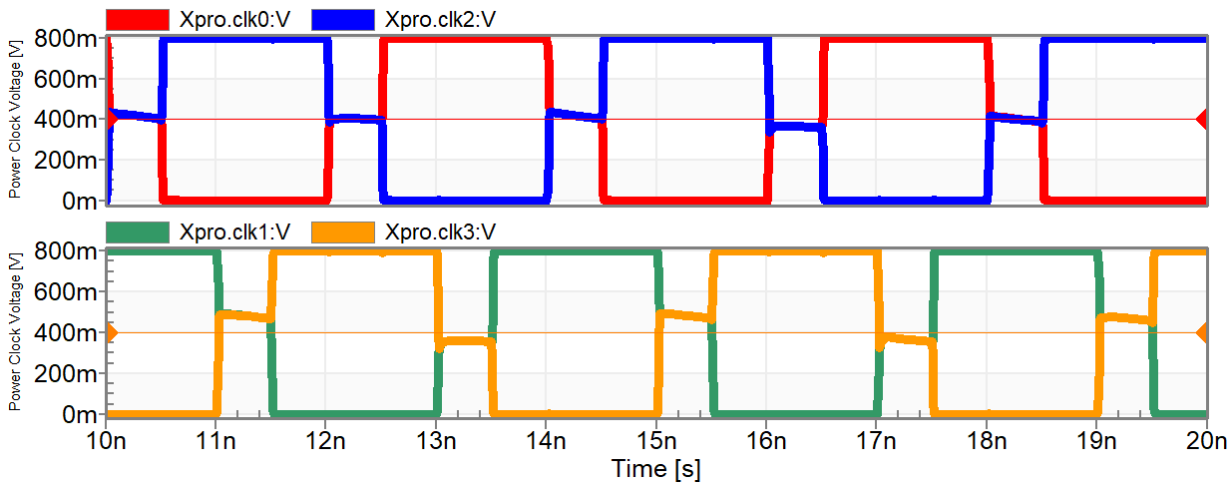


Figure 10. Power clock waveforms for the proposed stepwise charging driver circuit at 500 MHz adiabatic logic operation. **Upper plot:** ϕ_0 (red) and ϕ_2 (blue) can be seen to have relatively equal load as both their step voltages follow closely to half the supply voltage. **Lower plot:** ϕ_1 (green) and ϕ_3 (orange) show mismatched load as their step voltages deviate from half the supply. An analysis of the unloaded outputs of ϕ_3 in Figure 7 show this to be the case, with only the self-loading of the logic gates present for that power clock.

7. Conclusions

A novel stepwise charging driver circuit for four-phase adiabatic logic was designed and analyzed for power consumption compared to a standard CMOS and to a reference

step driver design. A series of simulations was performed using the FreePDK15 15 nm FinFET process comparing the two driver circuits. The proposed and reference drivers were both tasked with driving the same arbitrary logic function and both logical accuracy and power consumption were analyzed. These simulations were performed across a logical frequency range of 100 MHz to 1 GHz. Both drivers were able to drive the logic circuits for correct logical operation for each frequency tested. For the majority of the frequency range observed, both proposed and reference driver circuits operated within 1% power consumption of each other for the performance of adiabatic logic operations. However, the proposed driver circuit eliminates six transistors, six control signals, and four on-chip tank capacitors, leading to reduced circuit area requirements for the same circuit operation and efficiency.

Author Contributions: Conceptualization, W.M.; methodology, W.M.; software, W.M.; validation, W.M. and J.-W.C.; formal analysis, W.M.; investigation, W.M.; resources, W.M.; data curation, W.M. and J.-W.C.; writing—original draft preparation, W.M.; writing—review and editing, W.M. and J.-W.C.; visualization, W.M. and J.-W.C.; supervision, J.-W.C.; project administration, W.M. and J.-W.C.; funding acquisition, J.-W.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Dataset available on request from the authors.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Athas, W.; Svensson, L.; Koller, J. Low-Power Digital Systems Based on Adiabatic-Switching Principles. *IEEE Trans. Very Large Scale Integr. Syst.* **1994**, *2*, 398–407. [CrossRef]
2. Kuttappa, R.; Filippini, L.; Sica, N.; Taskin, B. Scalable Resonant power Clock Generation for Adiabatic Logic Design. In Proceedings of the IEEE Computer Society Annual Symposium on VLSI, Tampa, FL, USA, 7–9 July 2021.
3. Kuttappa, R.; Khoa, S.; Filippini, L.; Pano, V.; Taskin, B. Comprehensive Low Power Adiabatic Circuit Design with Resonant Power Clocking. In Proceedings of the 2020 IEEE International Symposium on Circuits and Systems, Seville, Spain, 12–14 October 2020.
4. Frank, M.; Brocato, R.; Conte, T.; Hsia, A.; Jain, A.; Missert, N.; Shukla, K.; Tierney, B. Special Session: Exploring the Ultimate Limits of Adiabatic Circuits. In Proceedings of the IEEE 38th International Conference on Computer Design, Hartford, CT, USA, 18–21 October 2020.
5. Jeanniot, N.; Pillonnet, G.; Nouet, P.; Azemard, N.; Todri-Sanial, A. Synchronised 4-Phase Resonant Power Clock Supply for Energy Efficient Adiabatic Logic. In Proceedings of the 2017 IEEE International Conference on Rebotting Computing, Washington, DC, USA, 8–9 November 2017.
6. Koller, J.G.; Svensson, L. Driving a capacitive load without dissipating fCV2. In Proceedings of the IEEE Symposium on Low Power Electronics, San Diego, CA, USA, 10–12 October 1994.
7. Raghav, H.S.; Bartlett, V.A.; Kale, I. Energy efficiency of 2-step charging power-clock for adiabatic logic. In Proceedings of the 2016 26th International Workshop on Power and Timing Modeling, Optimization and Simulation, Bremen, Germany, 21–23 September 2016.
8. Chernichenko, D.; Kushnerov, A.; Ben-Yaakov, S. Adiabatic charging of capacitors by Switched Capacitor Converters with multiple target voltages. In Proceedings of the 2012 IEEE 27th Convention of Electrical and Electronics Engineers in Israel, Eilat, Israel, 14–17 November 2012.
9. Khorami, A.; Saeidi, R.; Sharifkhani, M. An Analysis of Stepwise Adiabatic Circuits. In Proceedings of the 28th Iranian Conference on Electrical Engineering, Tabriz, Iran, 4–6 August 2020.
10. Raghav, H.S.; Bartlett, V.; Kale, I. Investigation of stepwise charging circuits for power-clock generation in Adiabatic Logic. In Proceedings of the 2016 12th Conference on Ph.D. Research in Microelectronics and Electronics, Lisbon, Portugal, 27–30 June 2016.
11. Moon, Y.; Jeong, D.-K. An efficient charge recovery logic. *IEEE J. Solid-State Circuits* **1996**, *31*, 514–522. [CrossRef]
12. Vetuli, A.; Pascoli, S.; Reyneri, L. Positive feedback in adiabatic logic. *Electron Lett.* **1996**, *32*, 1867–1869. [CrossRef]
13. FreePDK15. Available online: https://eda.ncsu.edu/freepdk15/ (accessed on 10 January 2024).